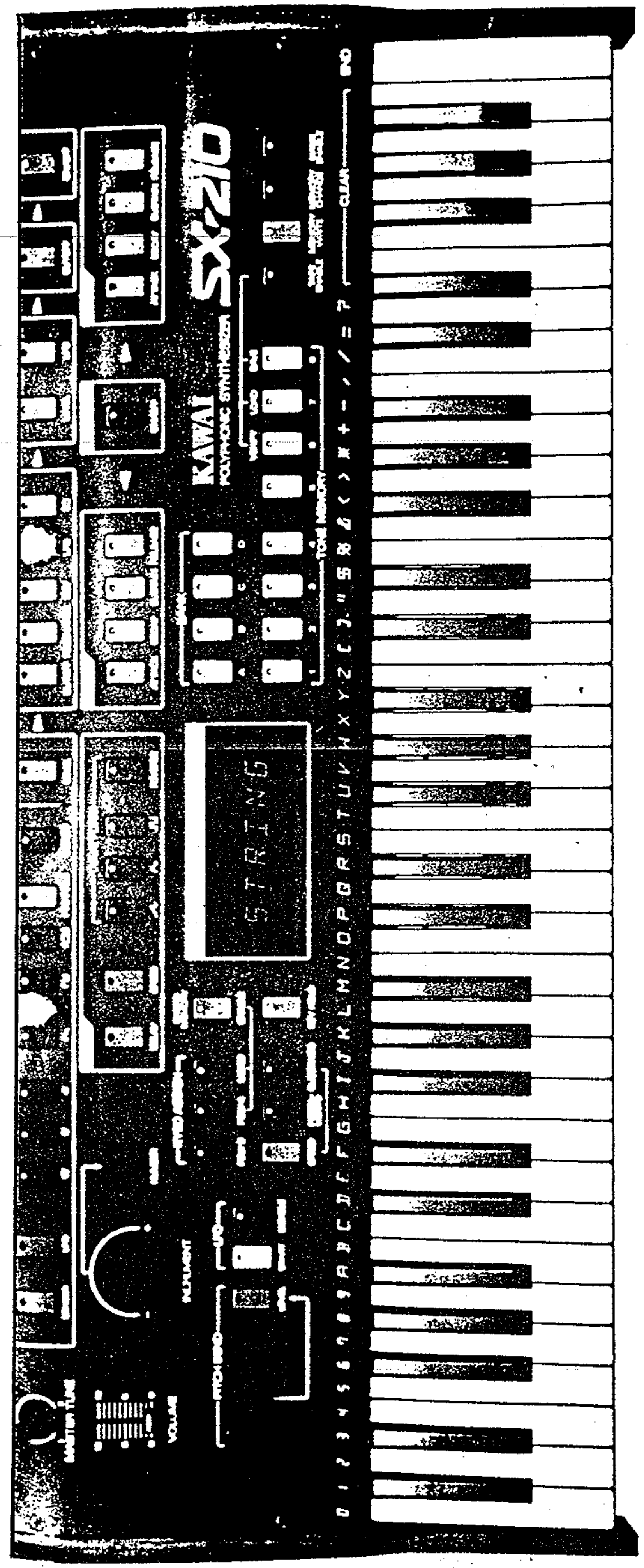
CONTENTS



KAWAI SX-210

8 VOICE POLYPHONIC PROGRAMMABLE SYNTHESIZER

Service Manual

KAWAI Kawai Musical Instrument Manufacturing Co., Ltd.

■ SPECIFICATIONS, PANEL LAYOUT

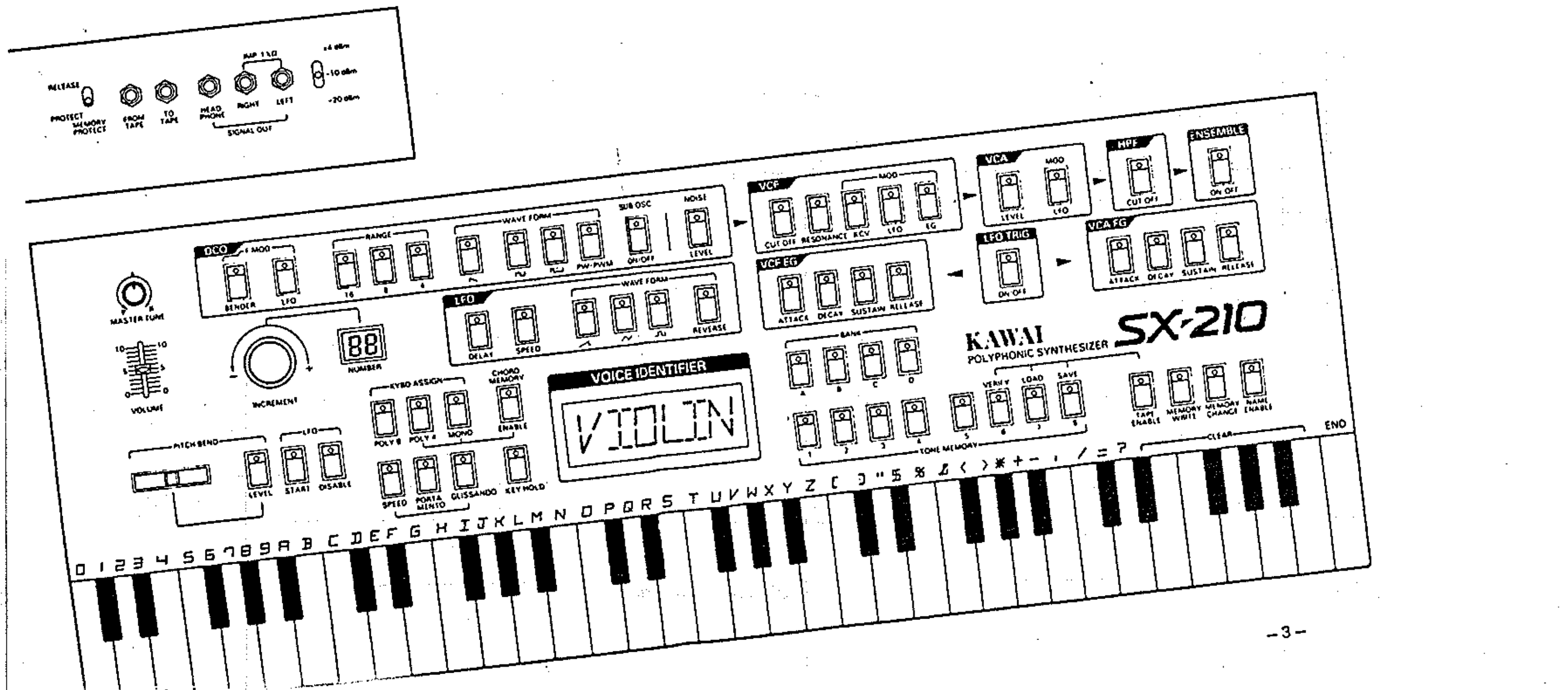
· SPECIFICATIONS

KEYBOARD		61 keys
DCO	Range	16' 8' 4'
	Wave Form	PW/PWM Mod.
	Frequency Modulation	Bend Depth LFO Mod. Depth
		Sub Osc
		Noise Level
KEYBOARD ASSIGN MODE		Poly 8 Poly 4 Mono Chord Memory
VCF		Cut-Off Frequency Resonance
	Modulation	KCV Mod. Depth LFO Mod. Depth EG Mod. Depth
VCA		Level
	Modulation	LFO Mod. Depth

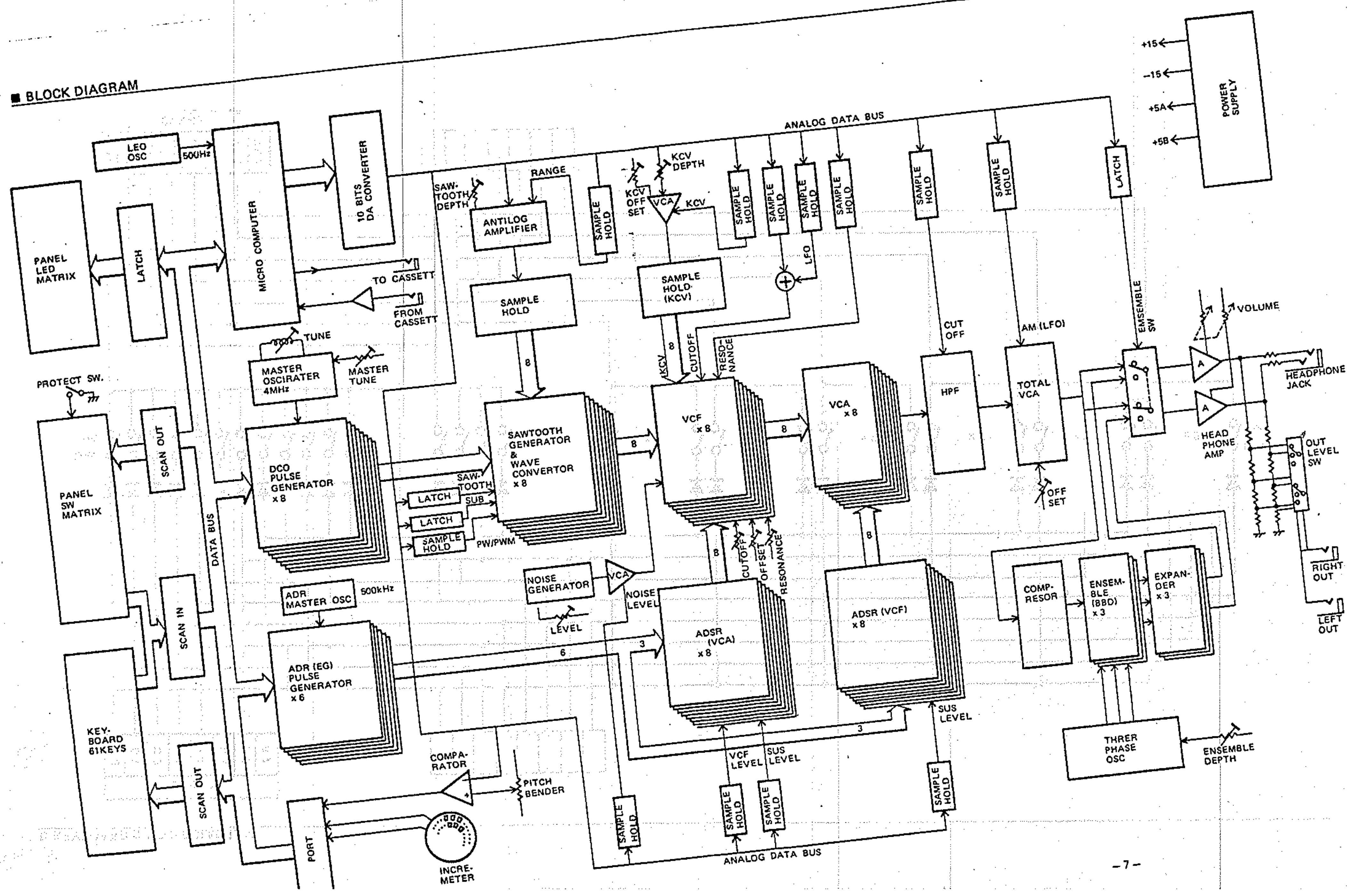
VCF-EG VCA-EG		Attack Time Decay Time Sustain Level Release Time
HPF		Cut-Off Frequency
LFO	Wave Form	
		Reverse
		Speed
		Delay Time
EFFECT		Ensemble
		Portamento Glissando
		Speed
		Hold
CONTROLLER	VCF-EG/VCA-EG	LFO Trigger
	Pitch Bender	Hand Controller Bend Depth
	LFO Modulation	Disable Start
		Total Volume
		Master Tune

MEMORY		Memory Write Memory Change Name Enable
VOICE IDENTIFIER		16 Segment LED x 6
INCREMENT NUMBER DISPLAY		7 Segment LED x 2
TAPE INTERFACE		Tape Enable Save Load Verify
REAR PANEL	Signal Out	Left Right Level Select Switch Headphone
	Tape Save & Load	To Tape From Tape
		Memory Protect Switch
POWER CONSUMPTION		40W
DIMENSIONS		880(W) x 400(D) x 128(H) m/m
WEIGHT		12.2 kg

PANEL LAYOUT



■ BLOCK DIAGRAM

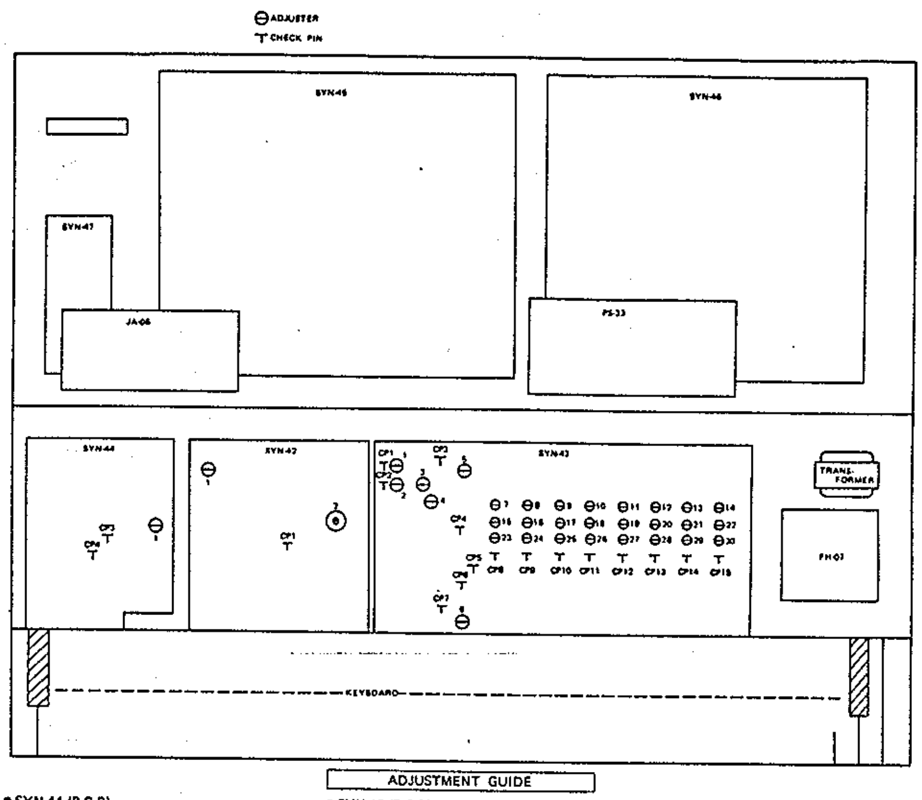


■ PRINTED CIRCUIT BORD GUIDE

PRINTED CIRCUIT BOARDS GUIDE

P.C.B. Name	Description	Page
SYN-42	Micro Computer	10
SYN-43	Sample and Hold, Noise Generator, Sawtooth Generator, Wave Form Converter, VCF, VCF-EG, VCA, VCA-EG, HPF	16
SYN-44	Ensemble & Headphone Amplifier	24
SYN-45	Panel (Left Half)	28
SYN-46	Panel (Right Half)	32
PS-33 FH-07	Power Supply & Line Filter	38
SYN-47 JA-06	Rear Panel (Jacks & Volume)	40

■ P.C.B. LAYOUT



ADJUSTMENT GUIDE

• SYN-44 (P.C.B)

No.	Description
1	ENSEMBLE DEPTH Adj.

• SYN-42 (P.C.B)

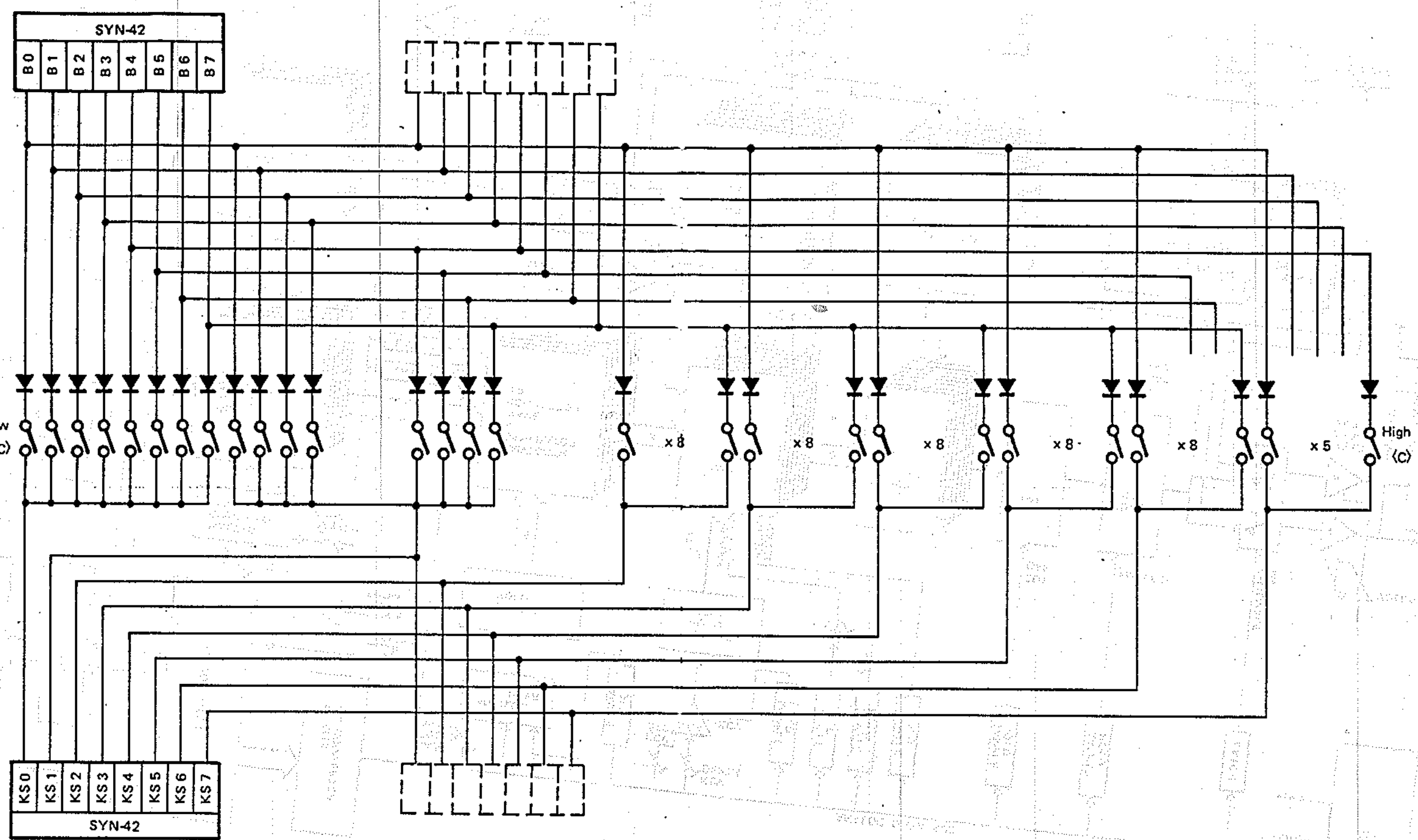
No.	Description
1	PITCH BEND Adj.
2	MASTER FINE TUNE

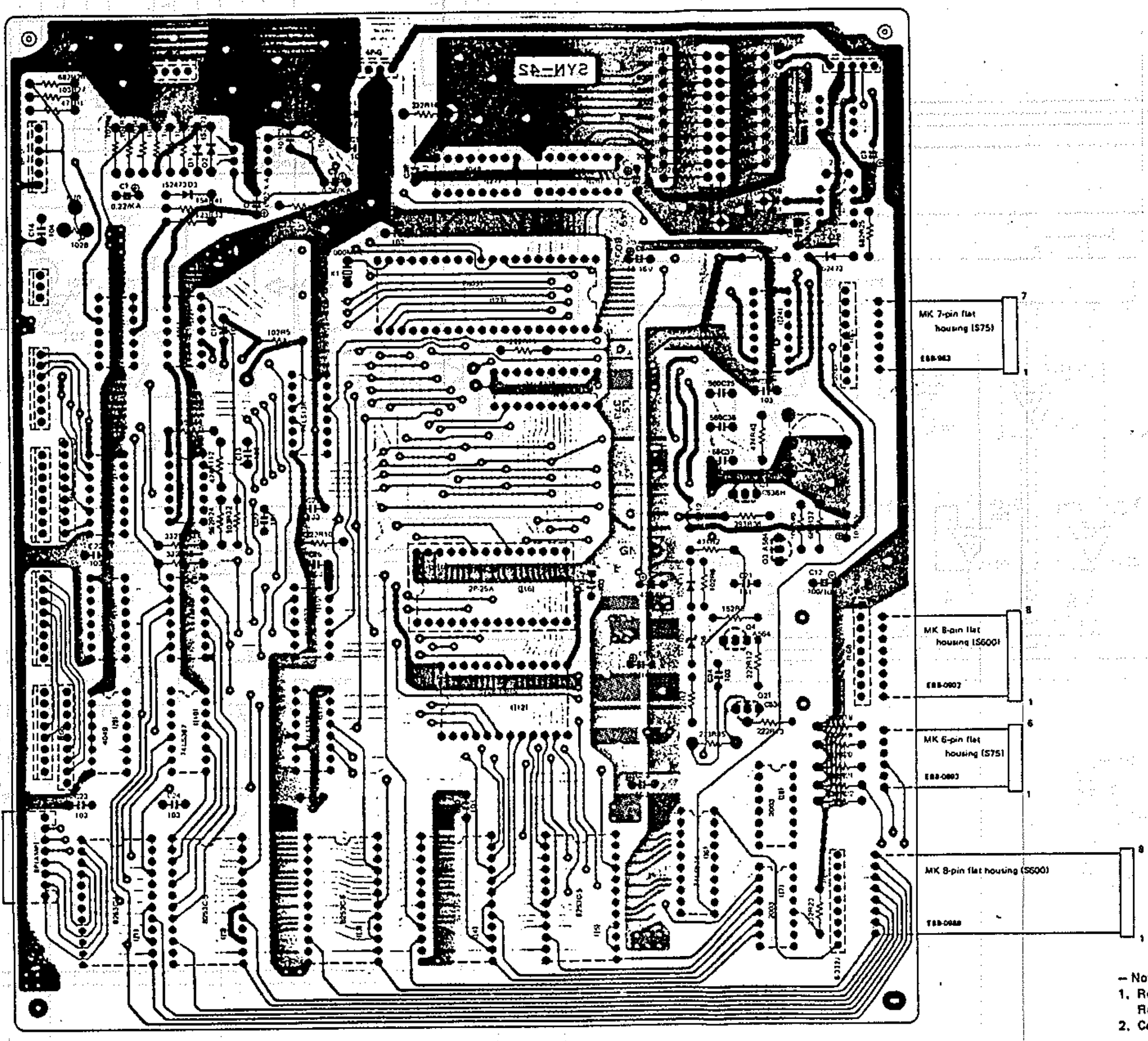
• SYN-43 (P.C.B)

No.	Description
1	ANTILOG OFFSET Adj.
2	TEMPERATURE COEFFICIENT Adj.
3	KCV LEVEL Adj.
4	KCV OFFSET Adj.
5	VCA OFFSET Adj.
6	NOISE LEVEL Adj.
7	VCF OFFSET (CH1) Adj.
8	VCF OFFSET (CH2)
9	VCF OFFSET (CH3)
10	VCF OFFSET (CH4)
11	VCF OFFSET (CH5)
12	VCF OFFSET (CH6)
13	VCF OFFSET (CH7)
14	VCF OFFSET (CH8)
15	VCF CUTOFF (CH1) Adj.
16	VCF CUTOFF (CH2)
17	VCF CUTOFF (CH3)
18	VCF CUTOFF (CH4)
19	VCF CUTOFF (CH5)
20	VCF CUTOFF (CH6)

No.	Description
21	VCF CUTOFF (CH7)
22	VCF CUTOFF (CH8)
23	VCF RESONANCE LEVEL (CH1)
24	VCF RESONANCE LEVEL (CH2)
25	VCF RESONANCE LEVEL (CH3)
26	VCF RESONANCE LEVEL (CH4)
27	VCF RESONANCE LEVEL (CH5)
28	VCF RESONANCE LEVEL (CH6)
29	VCF RESONANCE LEVEL (CH8)
30	VCF RESONANCE LEVEL (CH8)

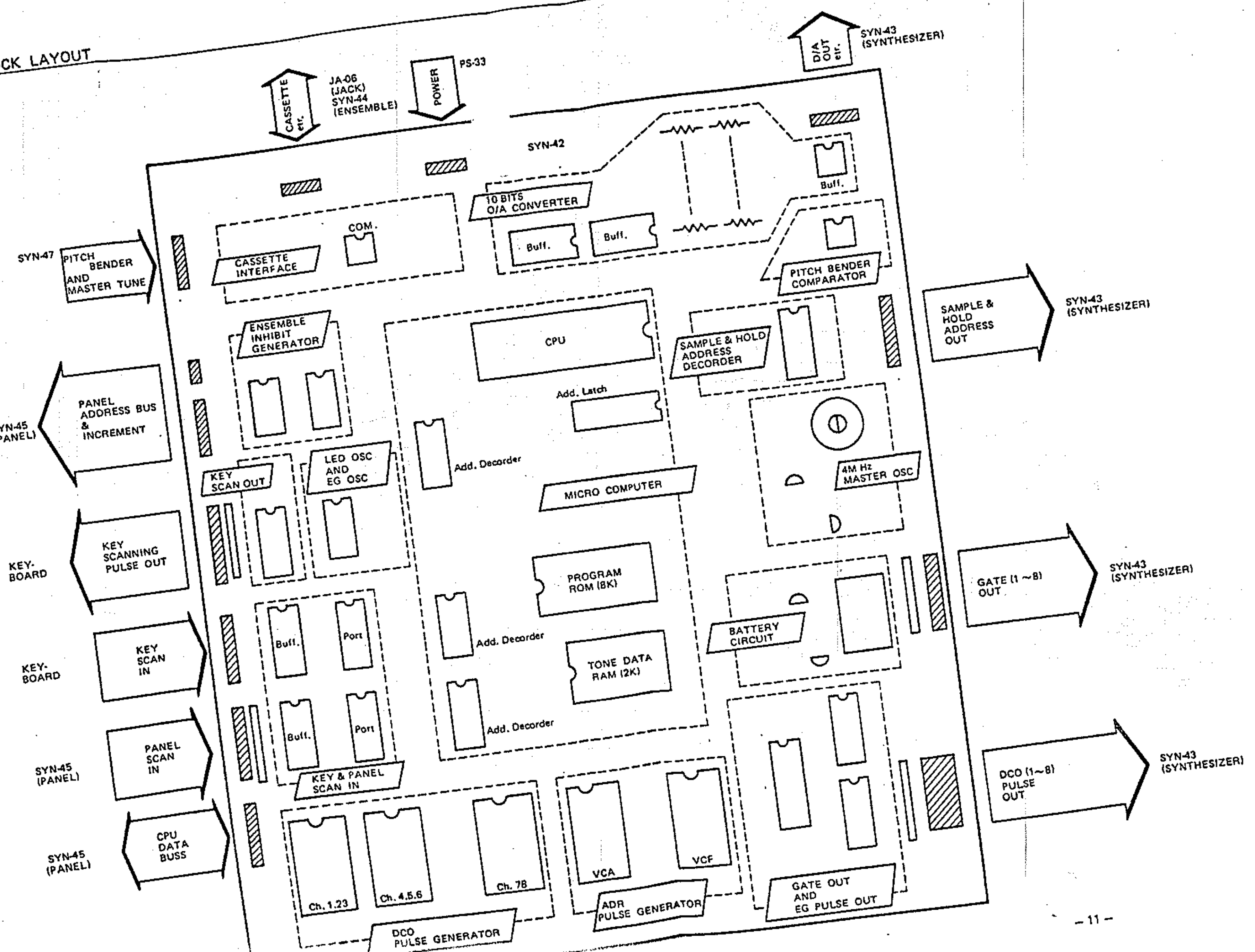
■ KEYBOARD CIRCUIT DIAGRAM



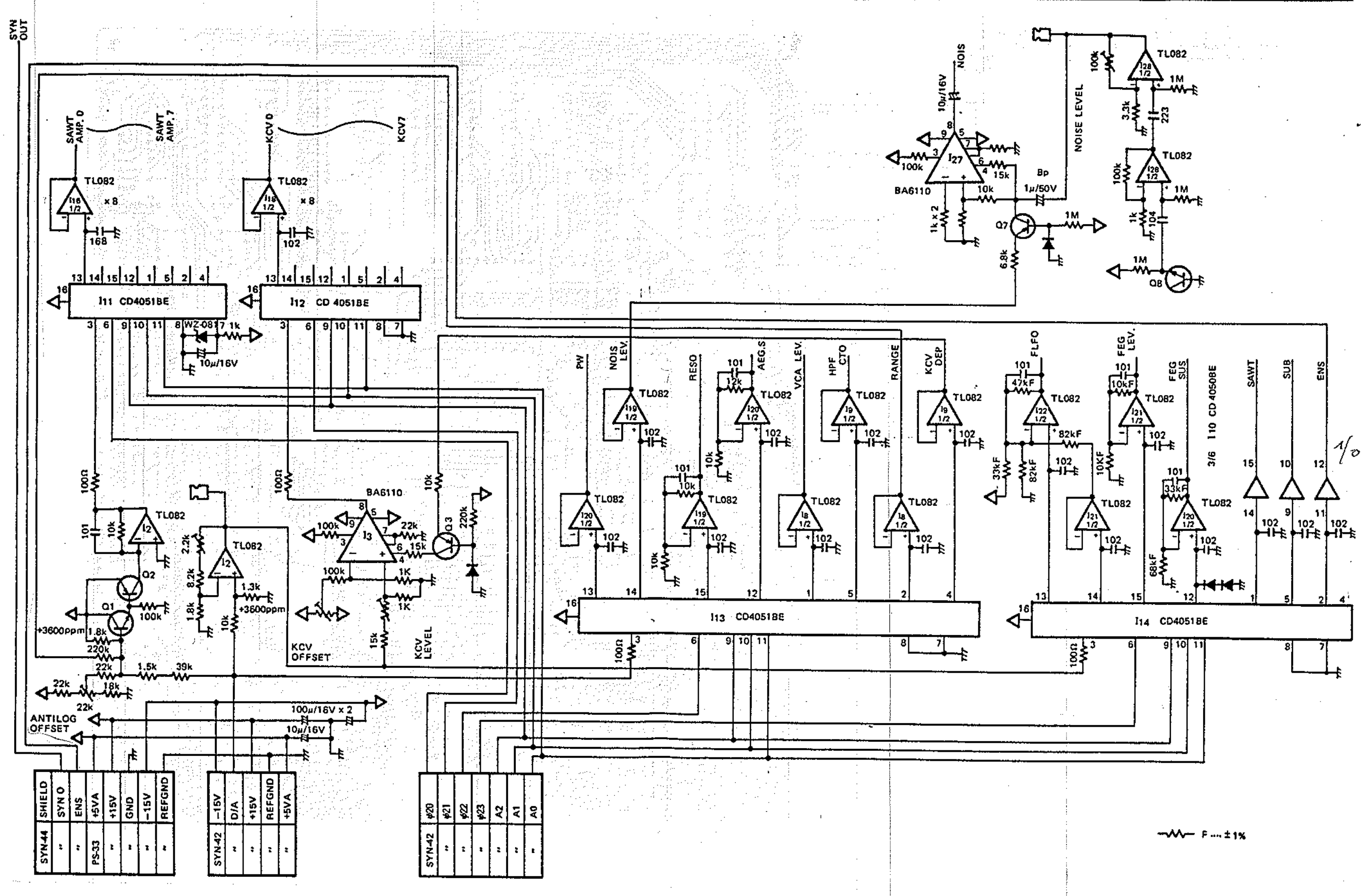


– Notes –
1. Resistors R45-48 (green 5th band) should be accurate to within 0.5%. Resistors R49-64 (brown 5th band) should be accurate to within 1%.
2. Ceramic condensors C35-37 are all Part No. 800163.

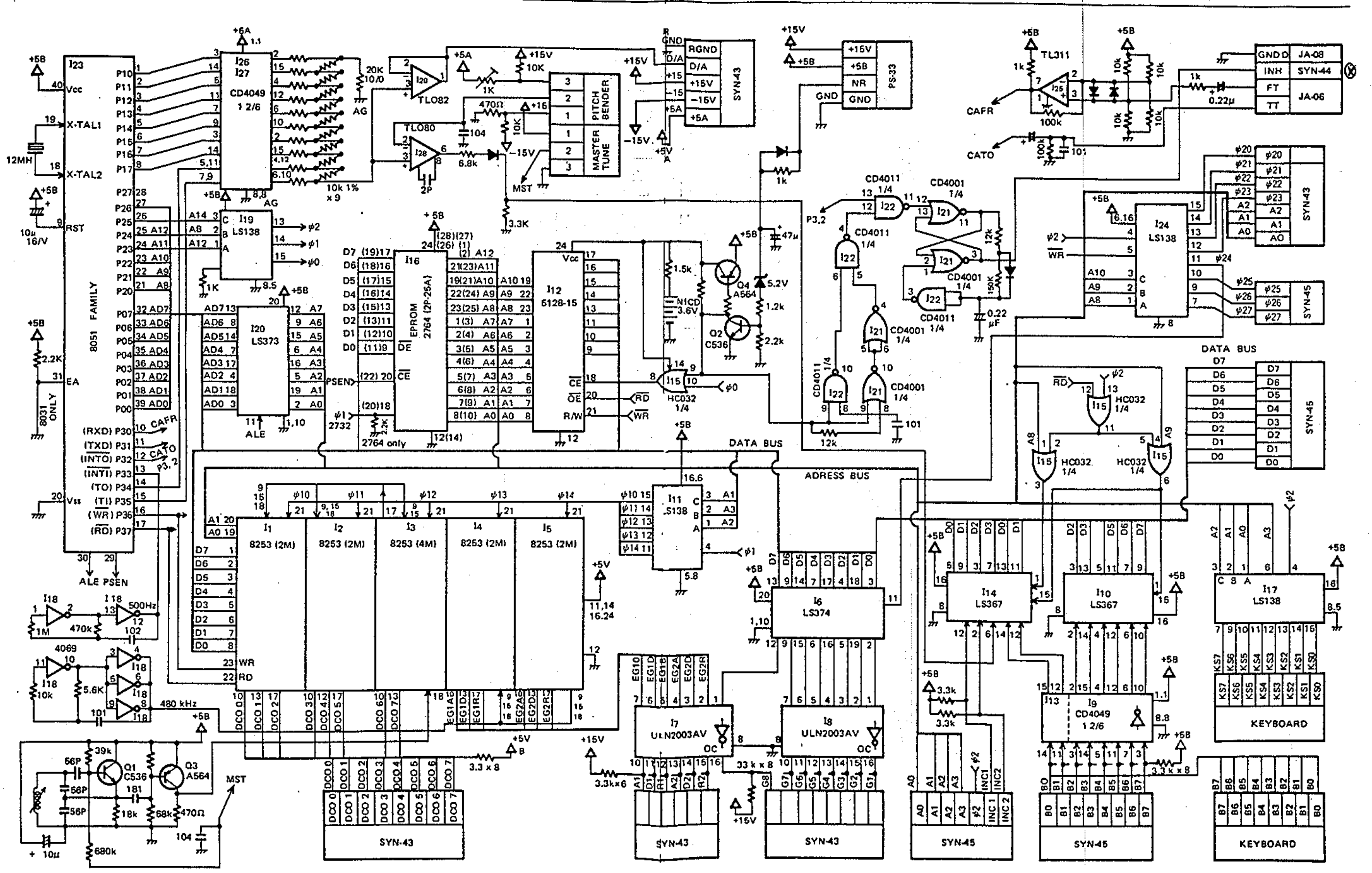
■ SYN-42 CIRCUIT BLOCK LAYOUT



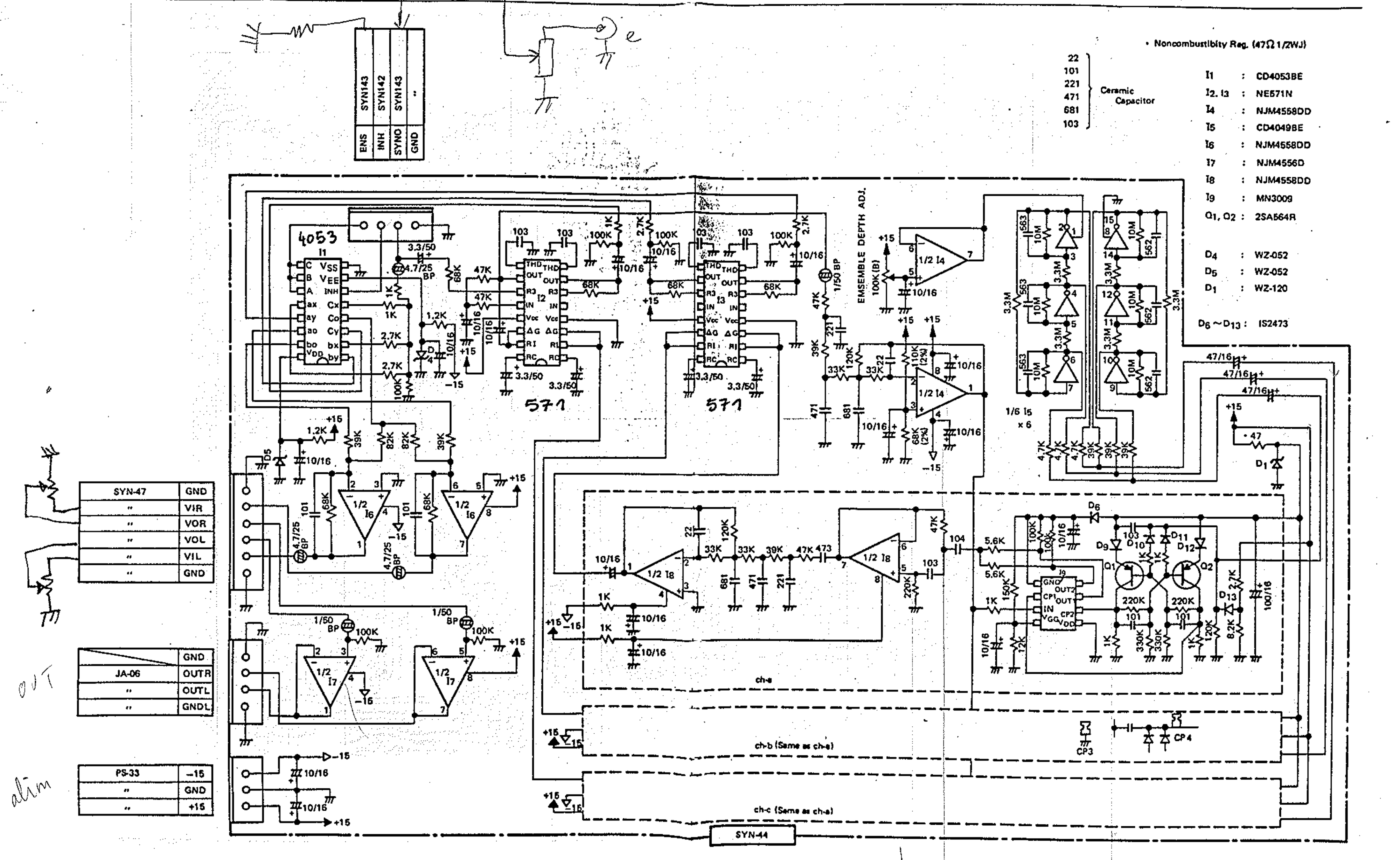
■ SYN-43 (1/2) CIRCUIT DIAGRAM SAMPLE AND HOLD, NOISE GENERATOR



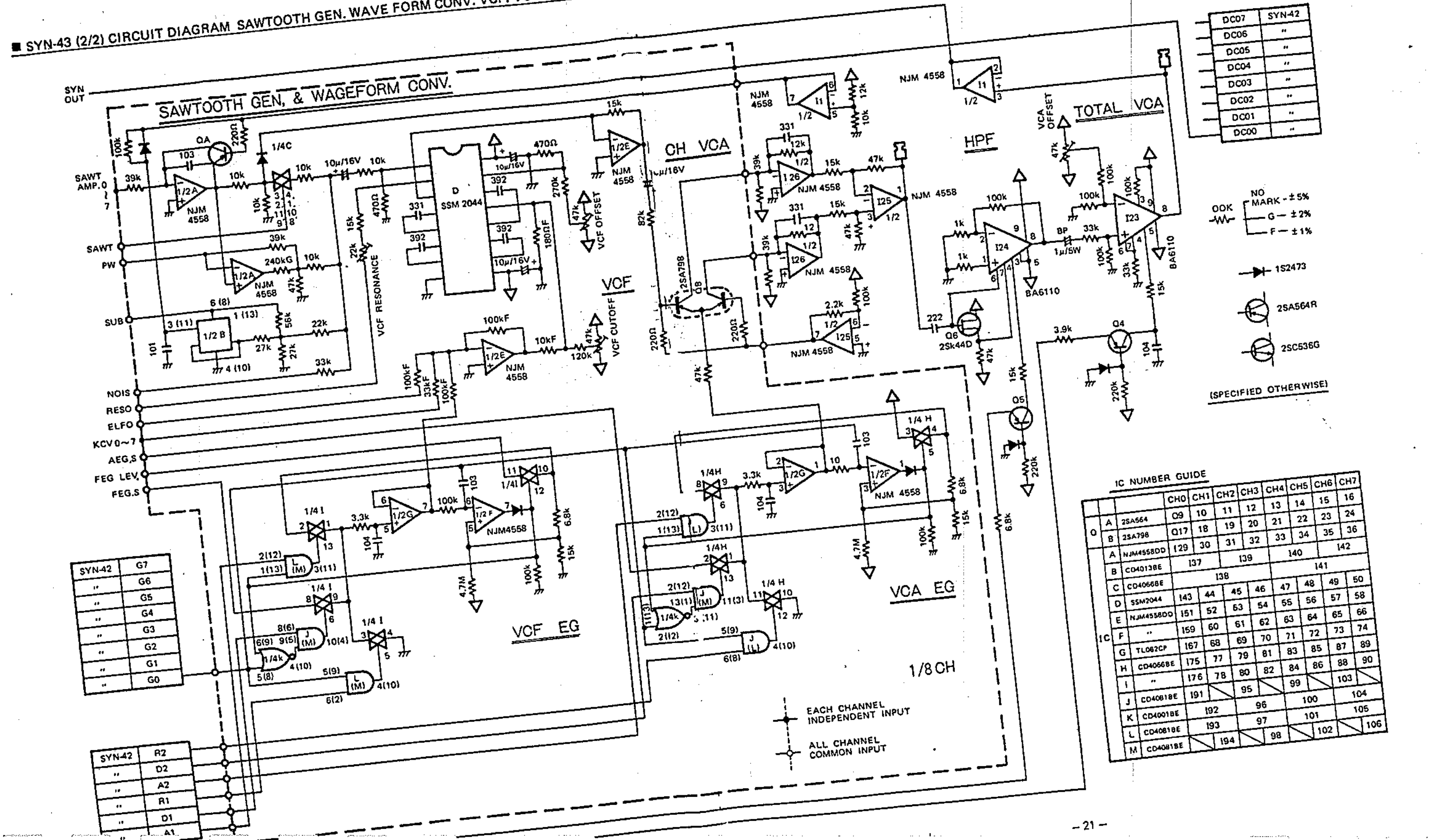
■ SYN-42 CIRCUIT DIAGRAM MICRO COMPUTER



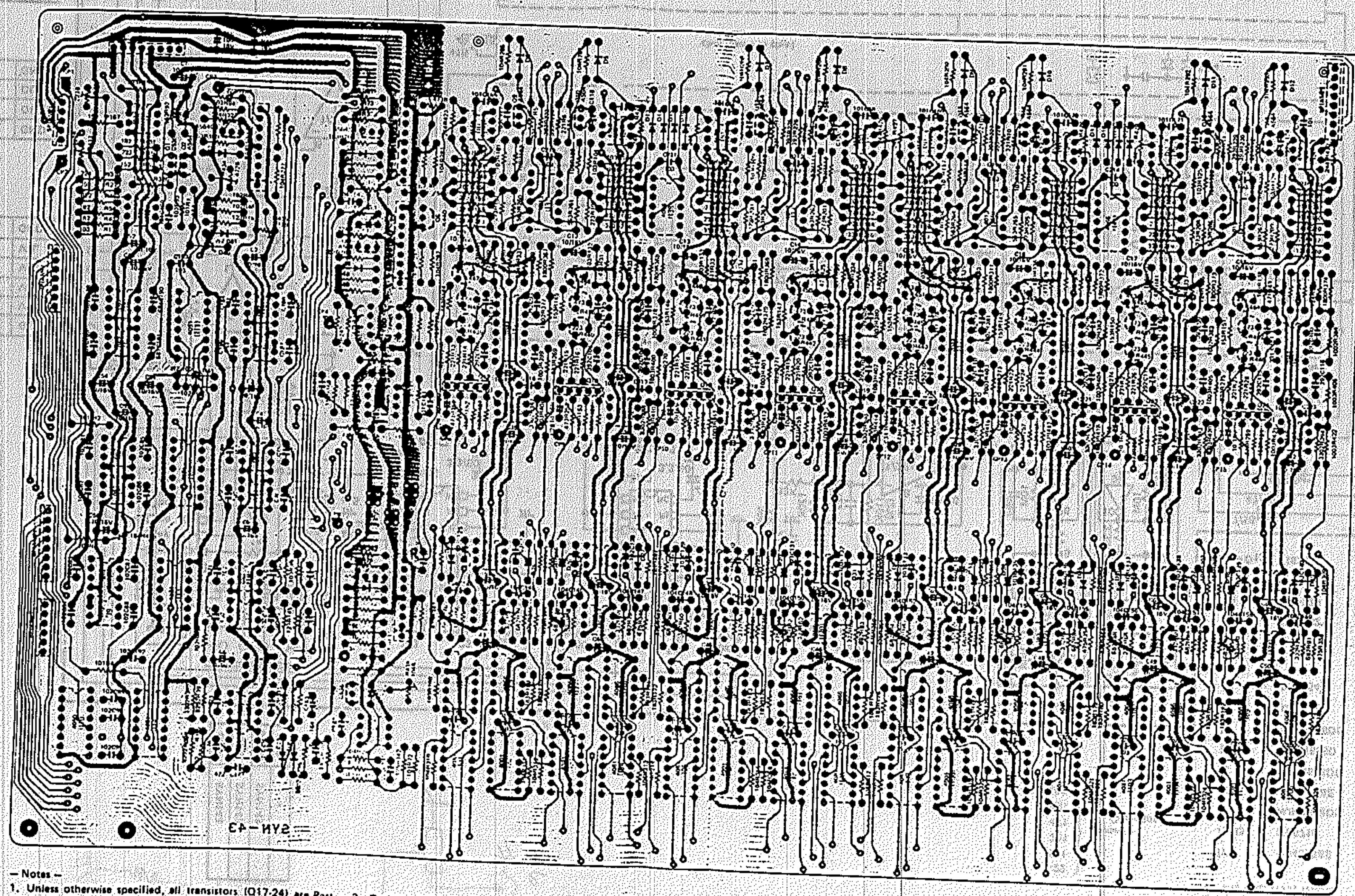
■ SYN-44 CIRCUIT DIAGRAM ENSEMBLE & HEADPHONE AMPLIFIER



■ SYN-43 (2/2) CIRCUIT DIAGRAM SAWTOOTH GEN. WAVE FORM CONV. VCF. VCFEG. VCAEG. HPF. VCA

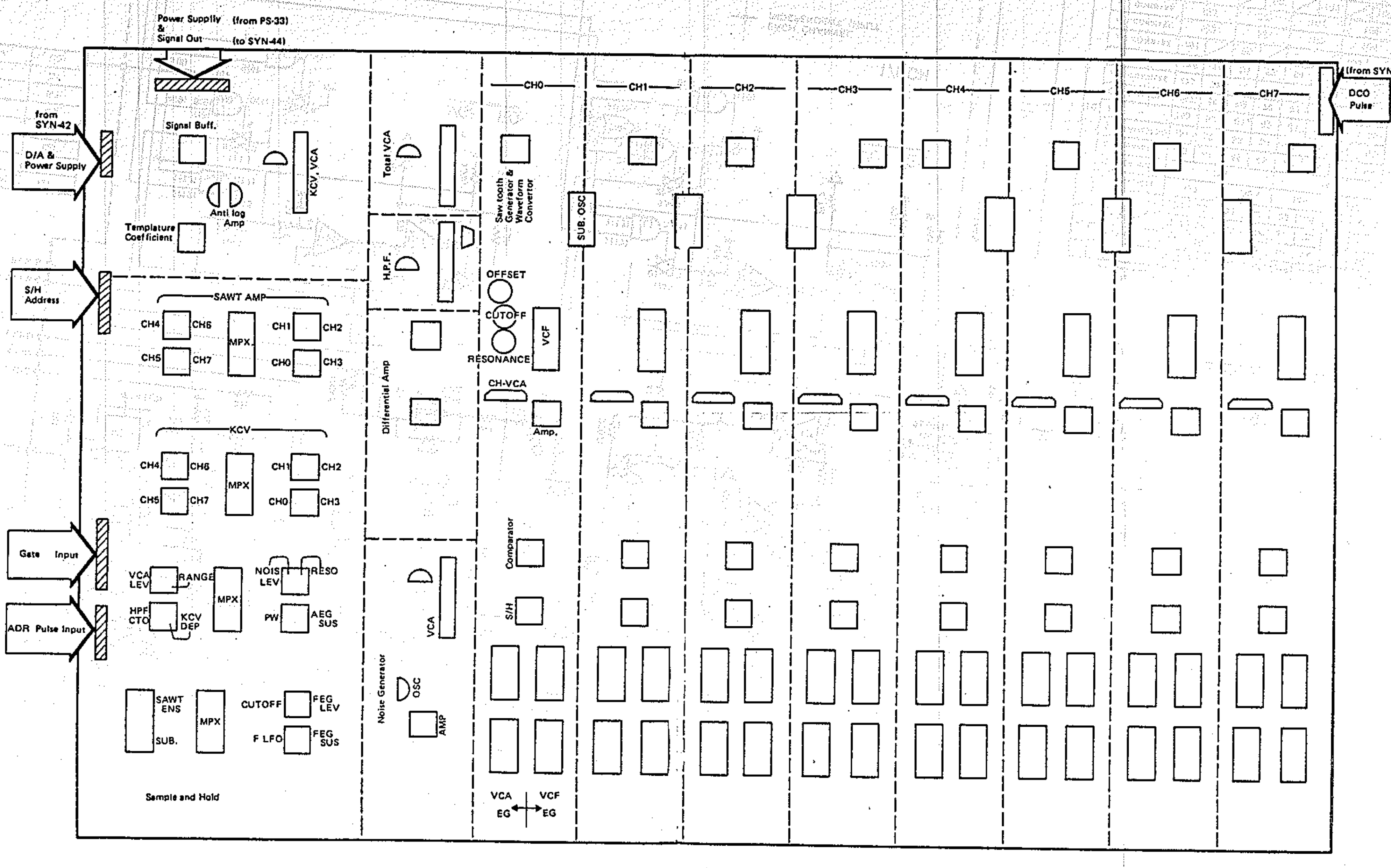


■ SYN-43

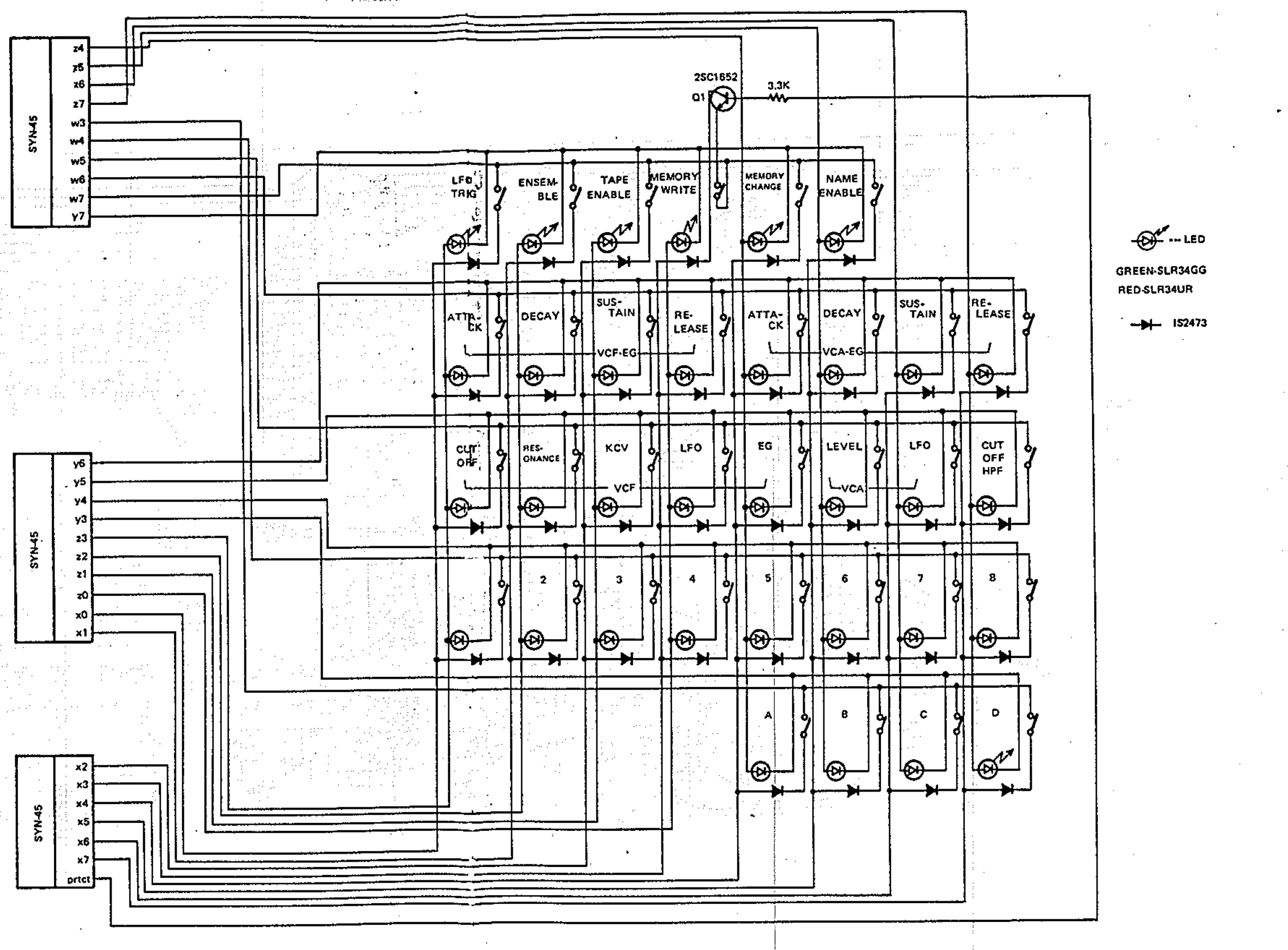


— Notes —
1. Unless otherwise specified, all transistors (Q17-24) are Part No. 2SA780.
2. Unless otherwise specified, all diodes are Part No. 1S2473.
3. Resistors R367-422 are metal-clad. (Tolerance: 1%)
Resistors R423-430 are carbon resistors. (Tolerance: 2%)
Resistors R431-432 are high-stability resistors.
4. Resistors R439-462 are semi-variable resistors, VR (Part No. H0651A).
5. Mylar condensors C216-223 are all Part No. 333.

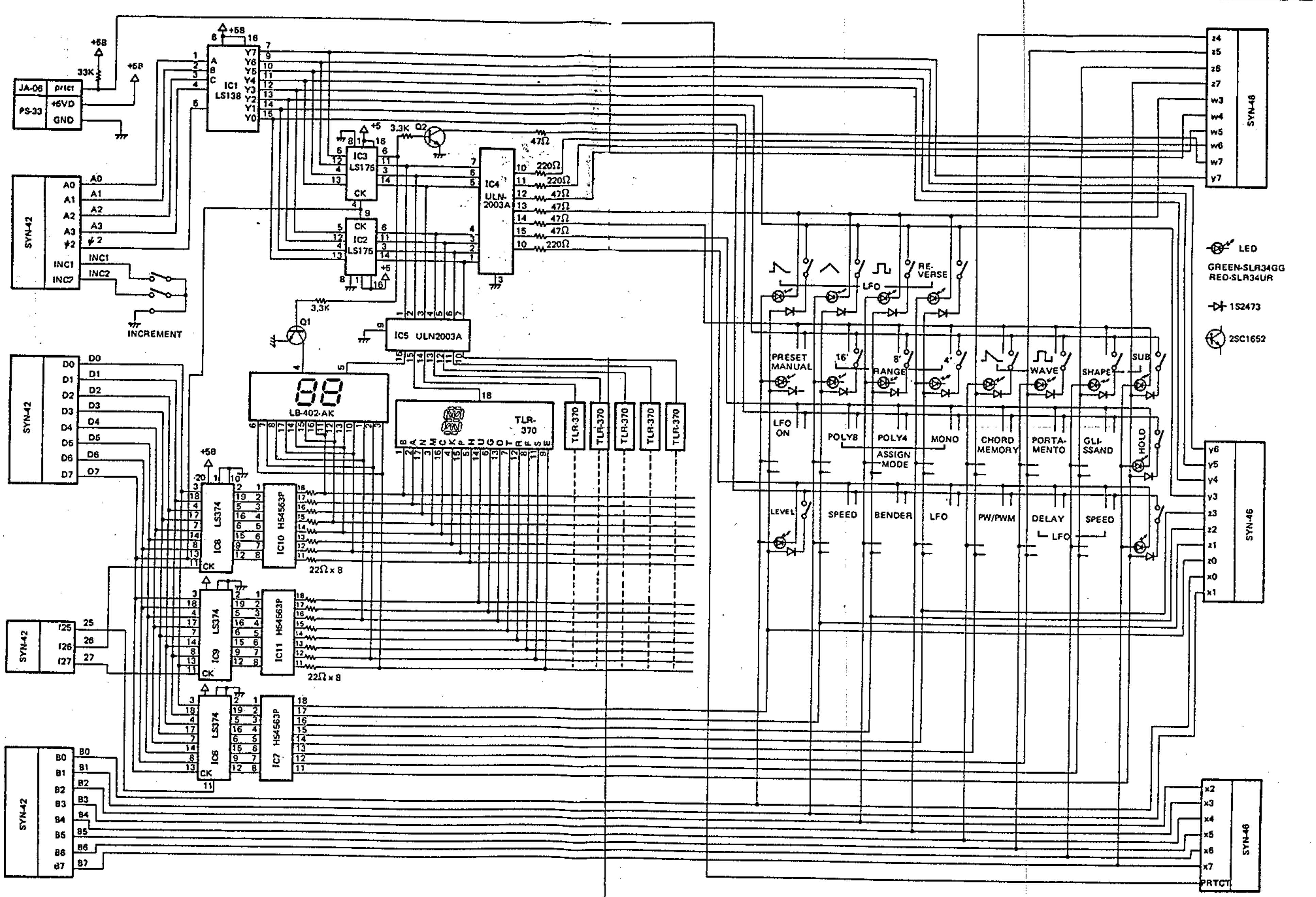
■ SYN-43 CIRCUIT BLOCK LAYOUT



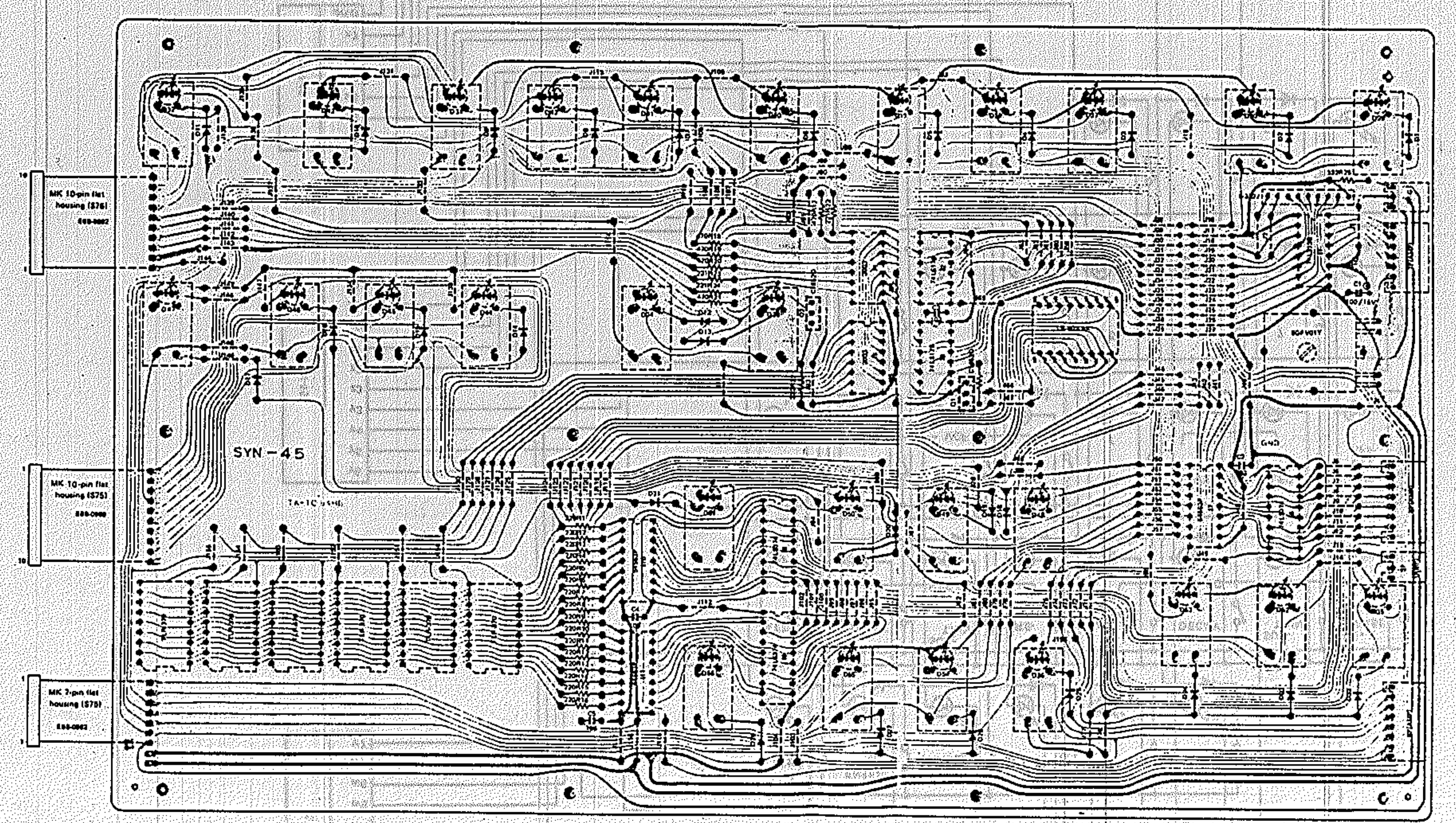
■ SYN-46 CIRCUIT DIAGRAM RIGHT HALF PANEL



■ SYN-46 CIRCUIT DIAGRAM LEFT HALF PANEL

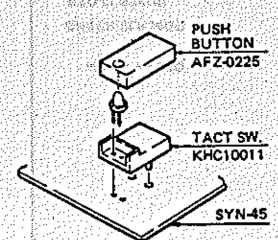


■ SYN-45

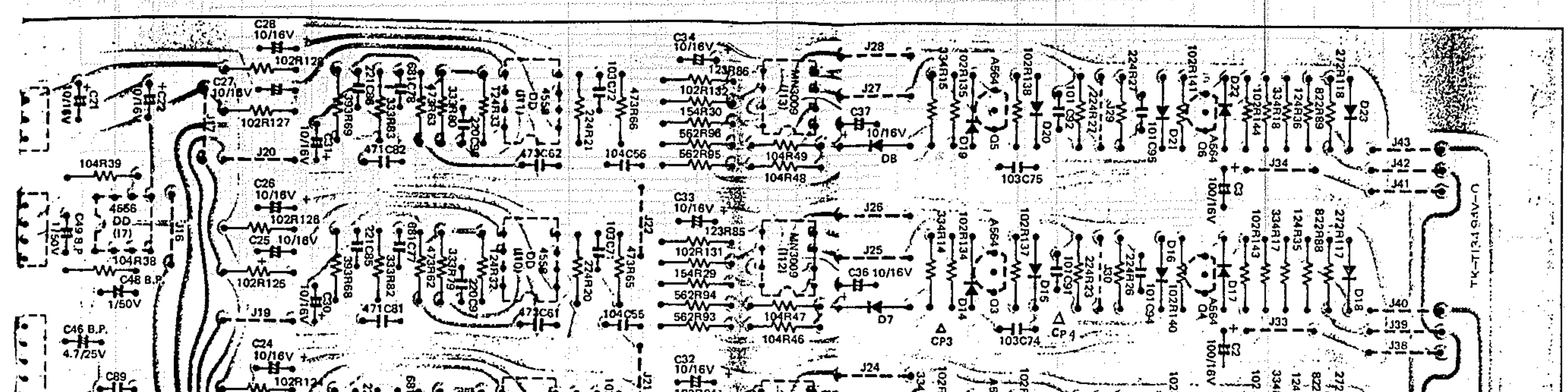


– Notes –

1. Unless otherwise specified, all diodes (D1-28) are Part No. 1S2473.
2. LEDs D29-36 are Part No. SLR-34UR. LEDs D37-56 are Part No. SLR-34GG.
3. Connecting leads J1-156 are 0.6 mm diameter, lead-plated wires.
4. SLR-34UR / SLR-34GG



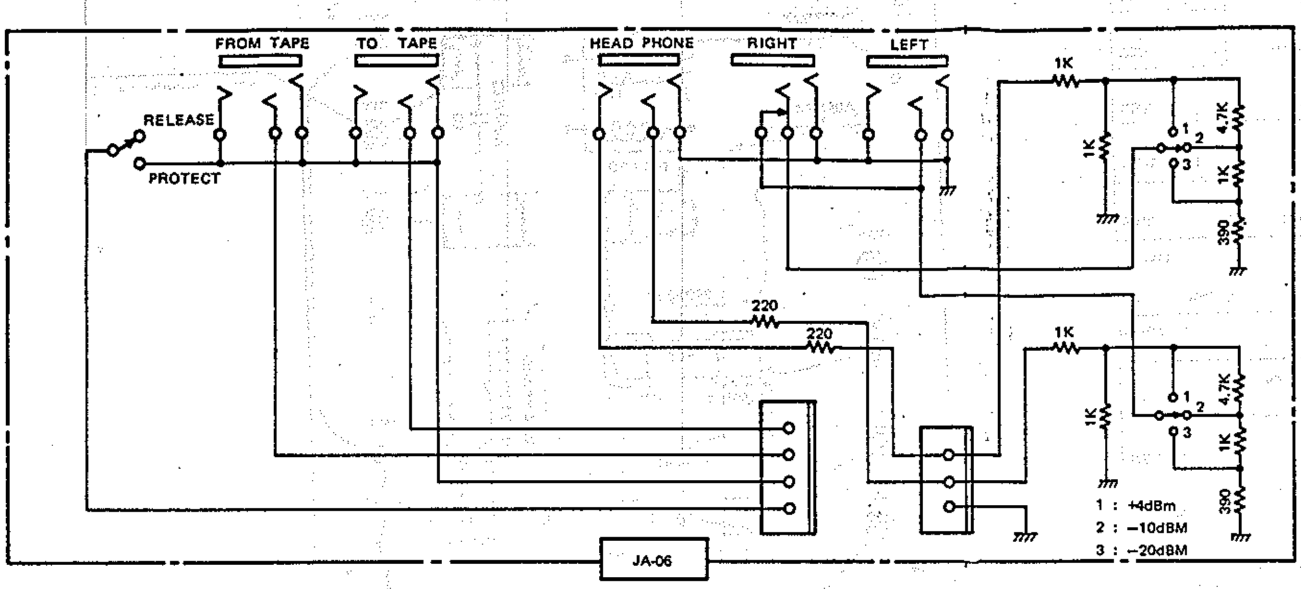
SYN-44



– Notes –

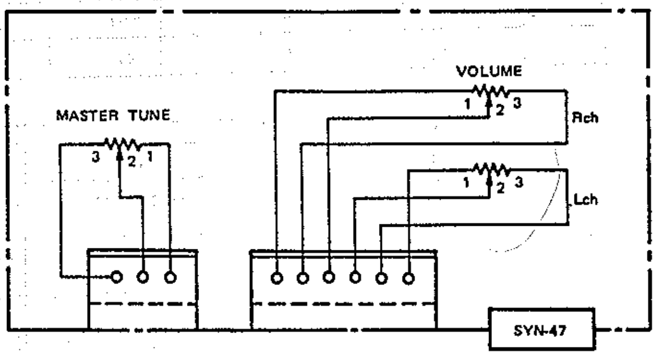
1. Diodes D4-5 are Part No. WZ-052. Unless otherwise specified, diodes (D6-23) are all Part No. 1S2473.
2. Connecting leads J1-55 are 0.6 mm diameter, lead-plated wires.
3. Carbon resistors R153-154 have tolerances of 2%.

■ JA-06 & SYN-47 JACKS & VOLUMES



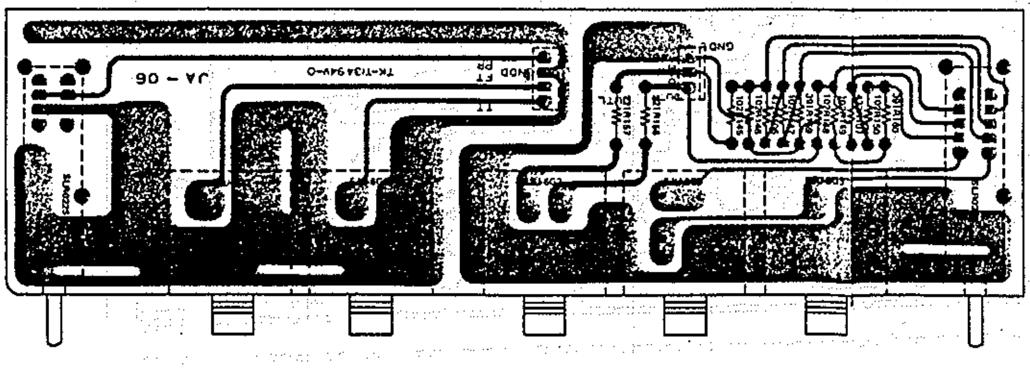
TT	SYN-42
FT	SYN-42
GND D	SYN-42
PR	SYN-45

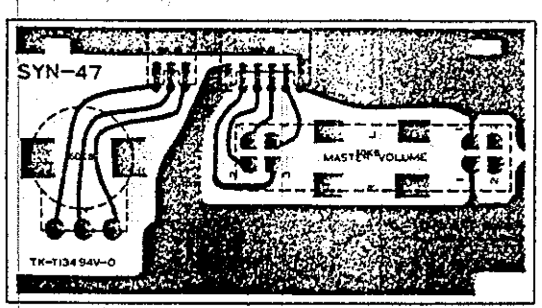
OUT R	SYN-44
OUT L	SYN-44
GND L	SYN-44



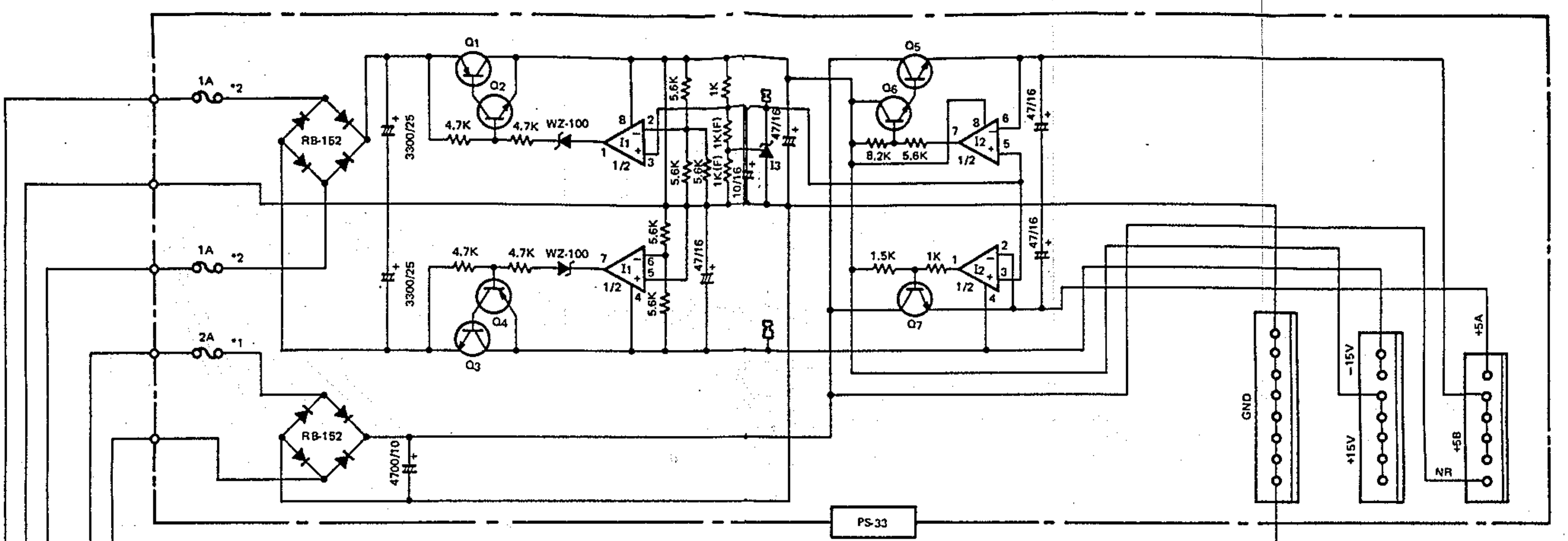
GND	MST	+15
SYN-42	SYN-42	SYN-42

GND	VIR	VOR	VOL	VIL	GND
SYN-47	SYN-47	SYN-47	SYN-47	SYN-47	SYN-47





■ PS-33 · FH-07 POWER SUPPLY & LINE FILTER

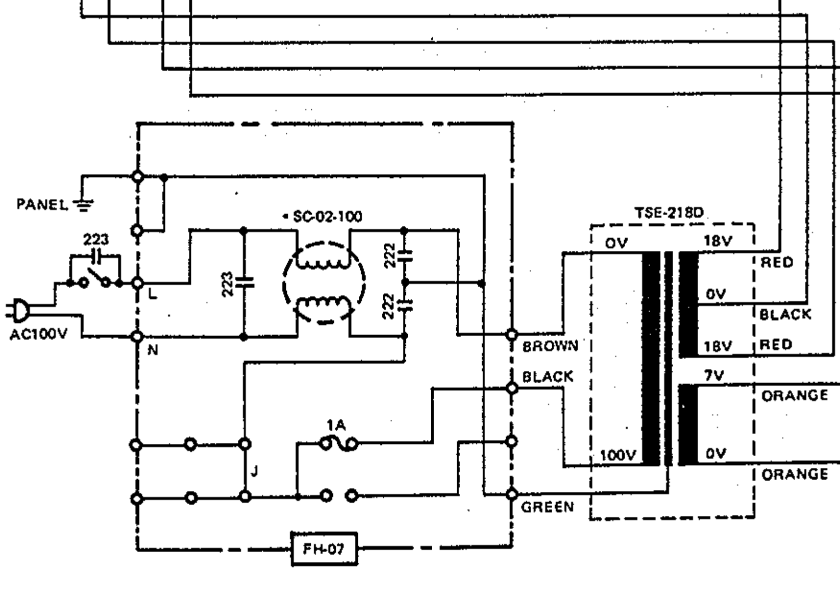


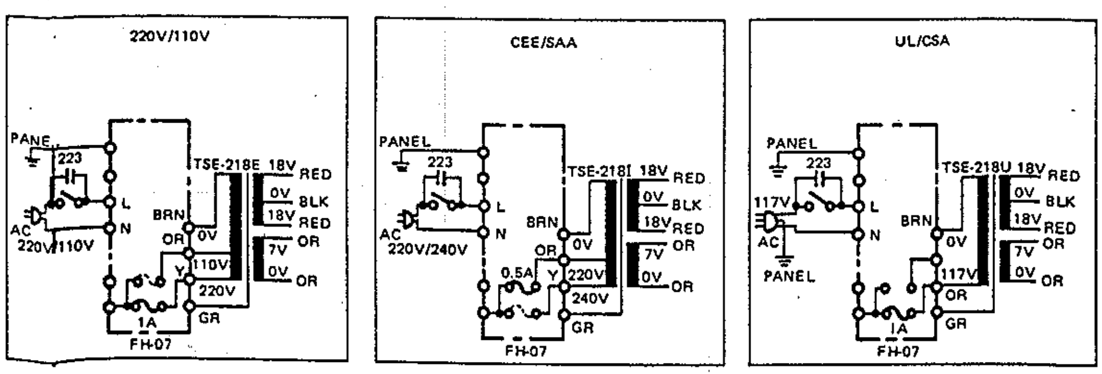
I₁, I₂ : NJM4558DD
I₃ : TL431C
Q₁ : 2SB941O
Q₂, Q₃ : 2SD1266Q
Q₅, Q₆, Q₇ : 2SC536F
Q₄ : 2SA564R

GND	SYN-43
"	"
"	SYN-42
"	SYN-44
"	SYN-45
"	
"	
"	PANEL

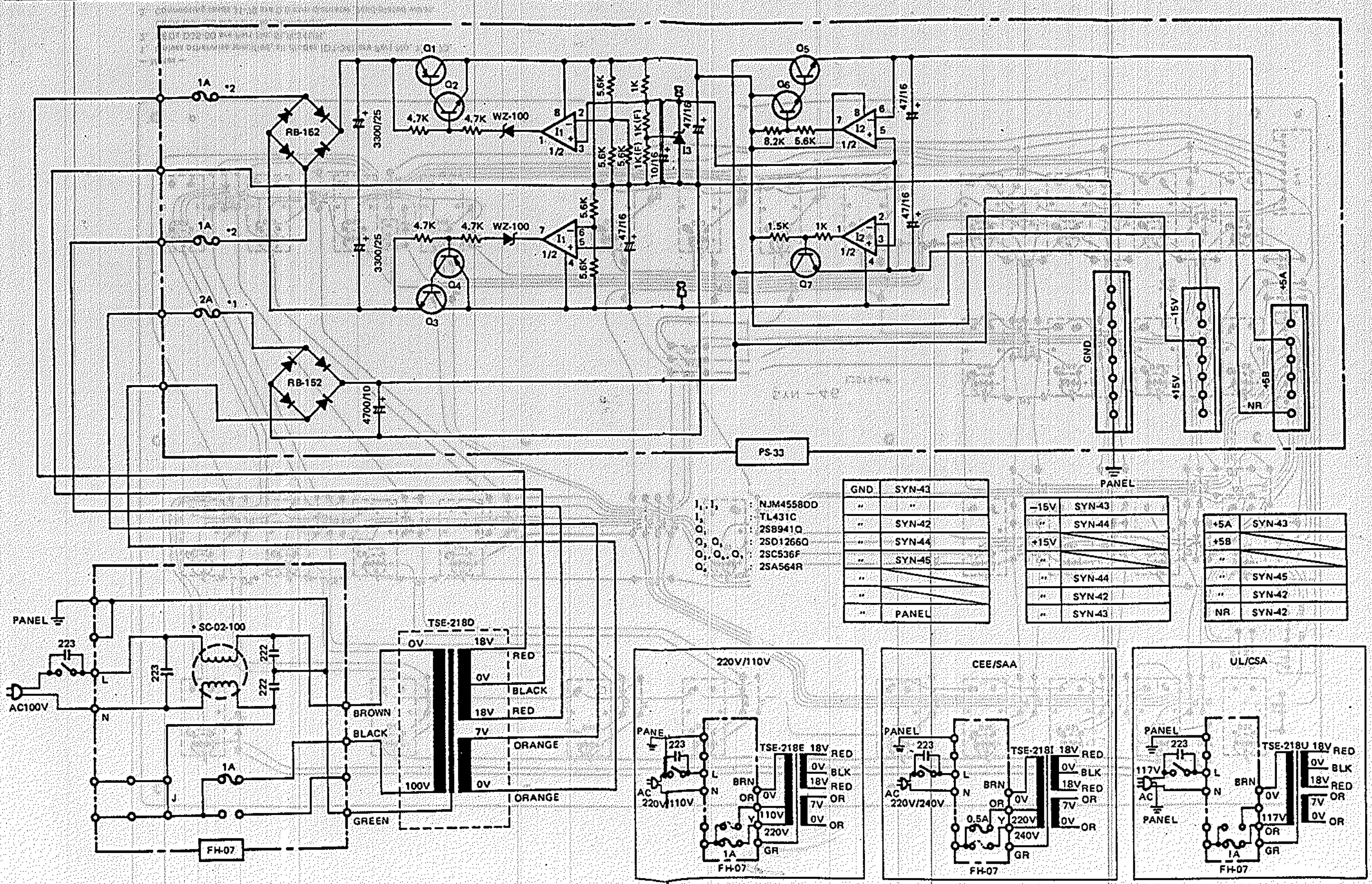
−15V	SYN-43
"	SYN-44
+15V	
"	
"	SYN-44
"	SYN-42
"	SYN-43

+5A	SYN-43
+5B	
"	
"	SYN-45
"	SYN-42
NR	SYN-42

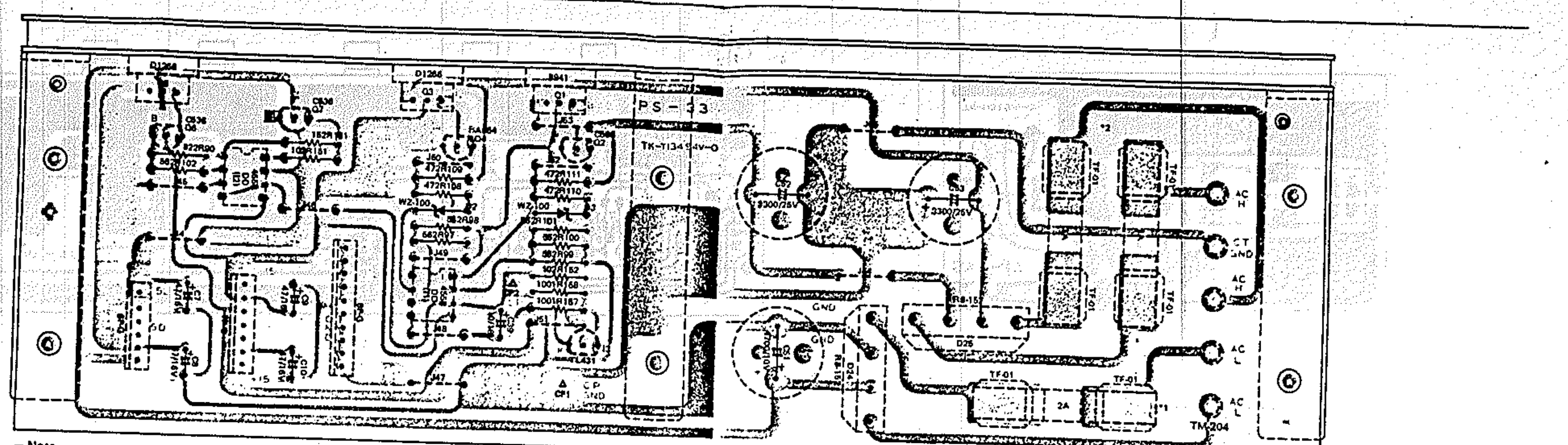




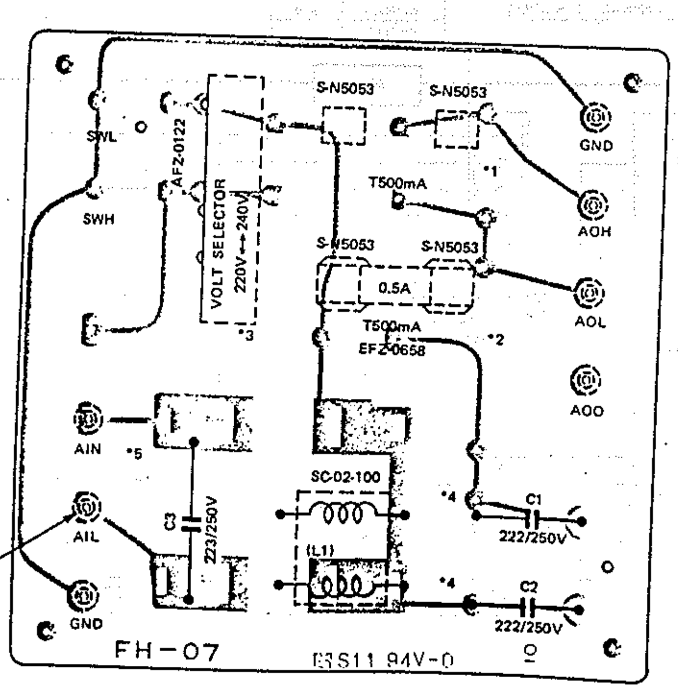
■ PS-33 · FH-07 POWER SUPPLY & LINE FILTER



■ PS-33 · FH-07



– Note –
Resistors R157-158 are metal-clad.



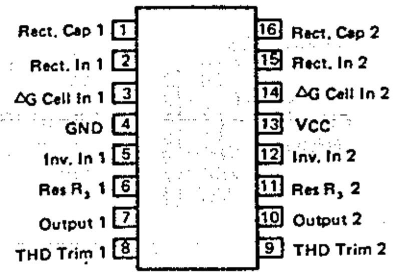
2. Pin terminal TM-204
X (7)

PS-33

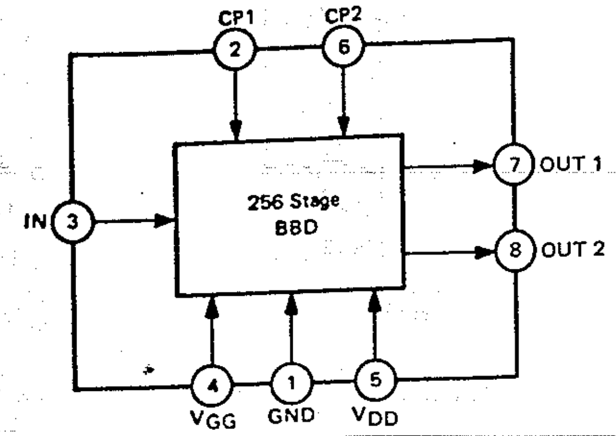
Market \ Item	*1 Fuse	*2 Fuse
CEE SAA	2A (5mm x 20mm)	1A (5mm x 20mm)
USA CSA	2A (6mm x 31mm)	1.5A (6mm x 31mm)
OTHERS	2A (6mm x 31mm)	1A (6mm x 31mm)

FH-07

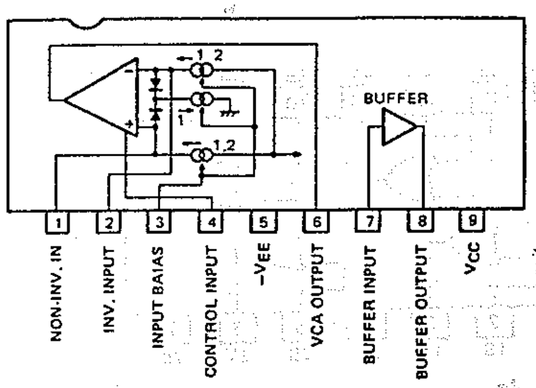
Market \ Item	*1 Fuse	*2 Fuse	*3 Seal	*4 Condenser	*5 Condenser
SAA	Not Use	0.5A (5mm x 20mm)	VOLT SELECTOR 220V ↔ 240V	222/250V (MP Condenser)	223/250V (MP Condenser)
NE·SE·CEE			Not Use		
USA	Seal	1.5A (6mm x 31mm)		222/125V	223/125V
CSA	Not Use				
JAPAN		1.25A (6mm x 31mm)		222/1000V	223/1000V
OTHERS	1A	Not Use	VOLT SELECTOR 220V ↔ 240V		



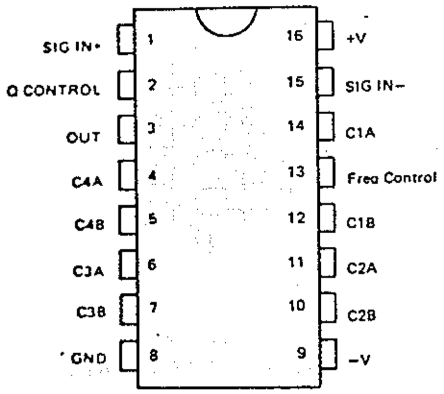
NE571N
COMPANDOR



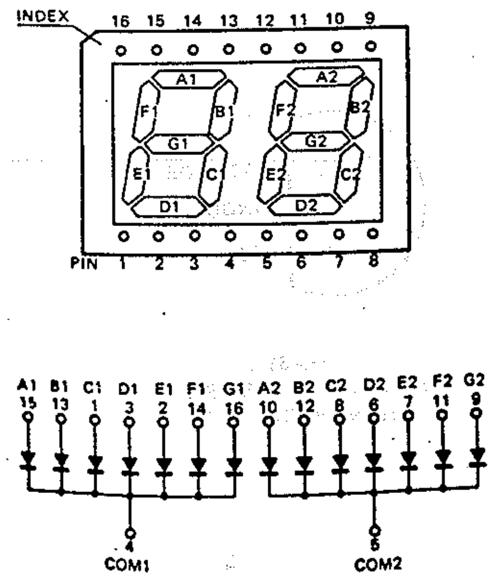
MN3009
256-STAGE BBD



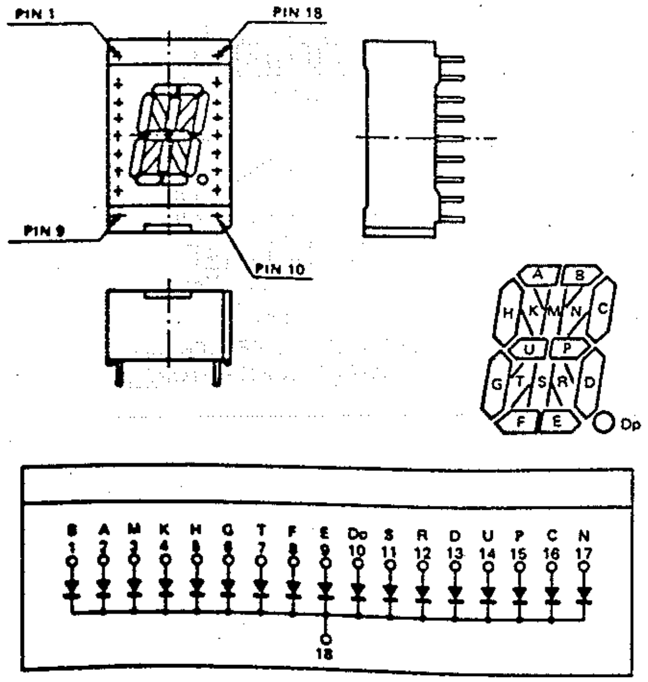
BA6110 V.C.A.



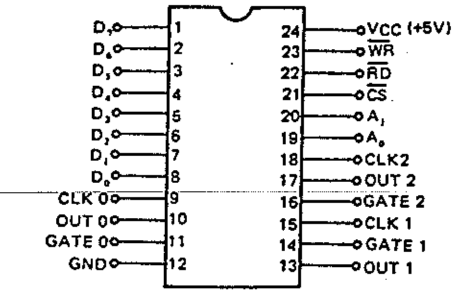
SSM 2044
4 POLE VOLTAGE CONTROLLED FILTER



LB-402

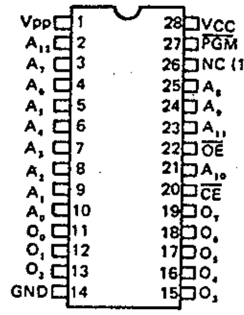


TLR-370



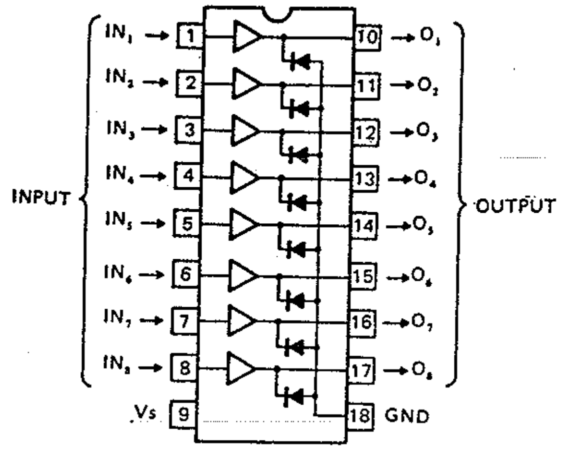
D_0 ~ D_7 : Data Bus (8 bit)
CLK N : Counter Clock Inputs
GATE N : Counter Gate Inputs
OUT N : Counter Output
$\overline{RD}$: Read Counter
$\overline{WR}$: Write Command or Date
$\overline{CS}$: Chip Select
A_0 ~ A_1 : Counter Select

µPD8253C-5
PROGRAMABLE INTERVAL TIMER

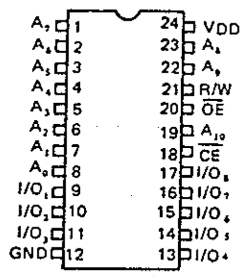


[1] For total compatibility and upgradability from the 2732A and ROMs provide a trace to pin 26.

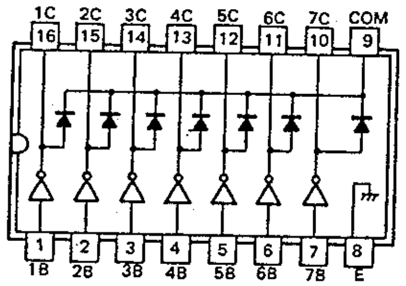
2764
(8K x 8) UV ERASABLE PROM



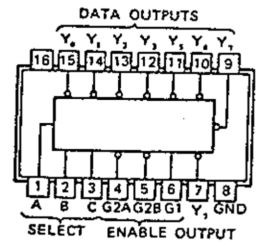
M54563P
8-UNIT 500mA SOURCE TYPE
DARLINGTON TRANSISTOR ARRAY



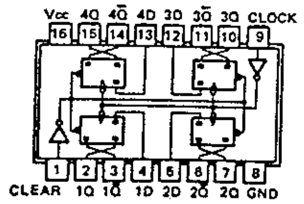
TC5517AP
(2048 x 8)
CMOS STATIC RAM
(or MSM 5128-15RS
or MB 8417A-15)



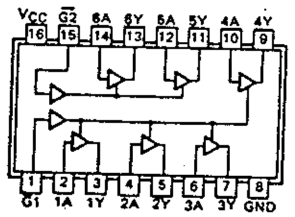
ULN2003A
DARLINGTON TRANSISTOR ARRAYS



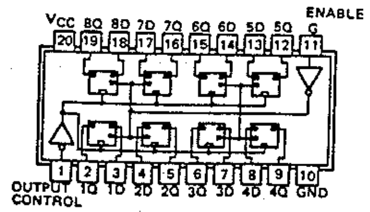
SN74LS 138
3-TO 8-LINE DECODERS/MULTIPLEXERS



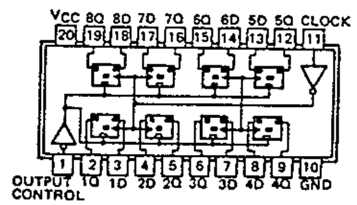
SN74LS 175
QUAD D-TYPE FLIP-FLOPS



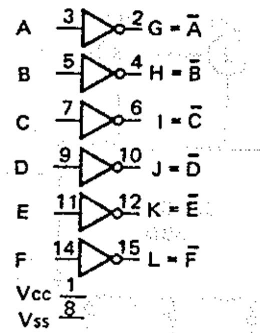
SN74LS 367
HEX BUS DRIVERS



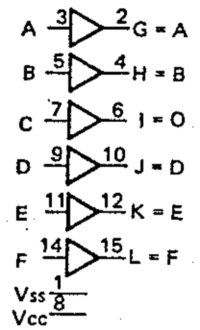
SN74LS 373
OCTAL D-TYPE LATCHES



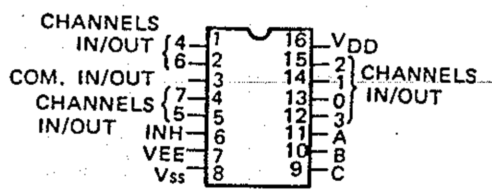
SN74LS 374
OCTAL D-TYPE FLIP-FLOPS



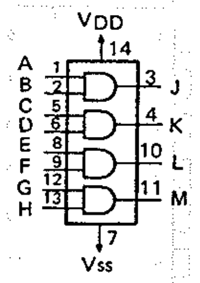
CD4049UB
HEX INVERTING BUFFERS



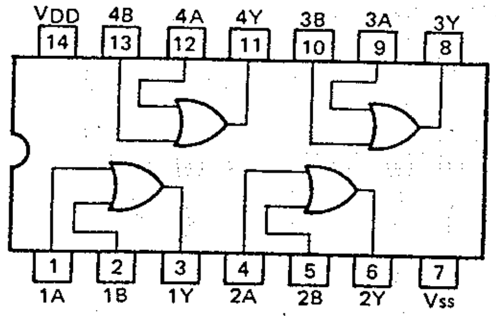
CD4050B
HEX NON-INVERTING BUFFERS



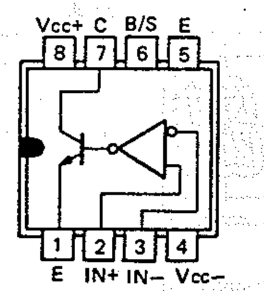
CD4051B
SINGLE 8-CHANNEL MULTIPLEXERS



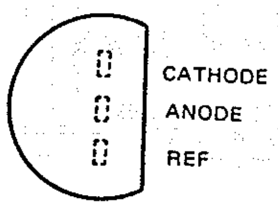
CD4081B
QUAD 2-INPUTS AND GATE



TC40H032
QUAD 2-INPUT OR GATE



TL311
JFET-INPUT DIFFERENTIAL COMPARATOR WITH STOROBE



TL431
ADJUSTABLE PRECISION SHUNT REGULATOR

8031
SINGLE-COMPONENT 8-BIT MICROCOMPUTER

■ 8031-Control Oriented CPU With RAM and I/O

- 4K x 8 ROM/EPROM
- 128 x 8 RAM
- Four 8-Bit Ports, 32 I/O Lines
- Two 16-Bit Timer/Event Counters
- High-Performance Full-Duplex Serial Channel
- External Memory Expandable to 128K
- Compatible with MCS-80 /MCS-85 Peripherals
- Boolean Processor
- MCS-48 Architecture Enhanced with:
  - Non-Paged Jumps
  - Direct Addressing
  - Four 8-Register Banks
  - Stack Depth Up to 128-Bytes
  - Multiply, Divide, Subtract, Compare
- Most Instructions Execute in 1μs
- 4μs Multiply and Divide

The Intel 8031/8051/8751 is a stand-alone, high-performance single-chip computer fabricated with Intel's highly-reliable +5 Volt, depletion-load, N-Channel, silicon-gate HMOS technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.
The 8051/8751 contains a non-volatile 4K x 8 read-only program memory; a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The 8031 is identical, except that it lacks the program memory. For systems that require extra capability, the 8051 can be expanded using standard TTL compatible memories and the byte oriented MCS-80 and MCS-85 peripherals.
The 8051 microcomputer, like its 8048 predecessor, is efficient both as a controller and as an arithmetic processor. The 8051 has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1μs, 40% in 2μs and multiply and divide require only 4μs. Among the many instructions added to the standard 8048 instruction set are multiply, divide, subtract and compare.

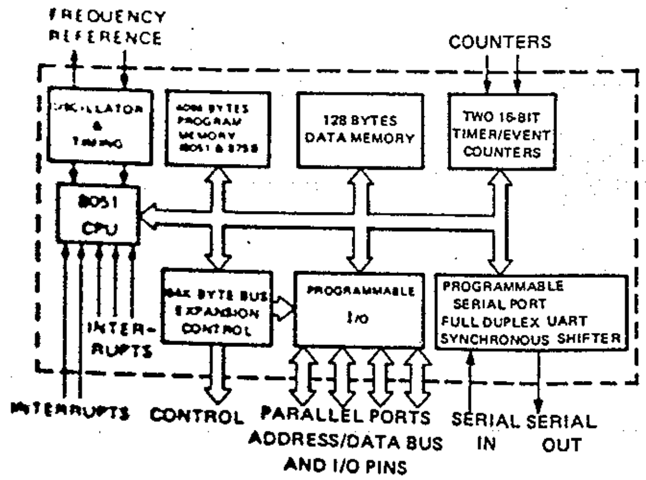


Figure 1.
Block Diagram

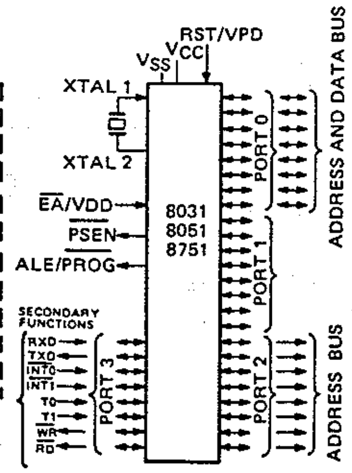


Figure 2.
Logic Symbol

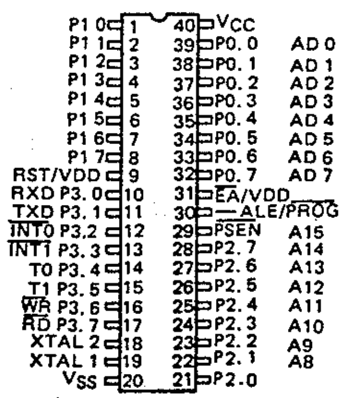
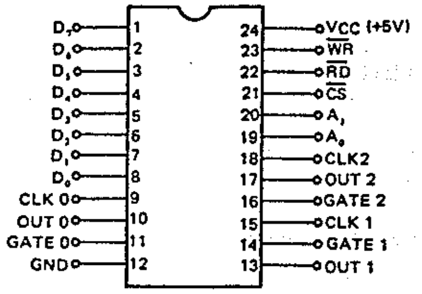


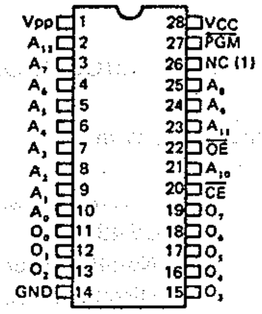
Figure 3.
Pin Configuration

■ I.C. INFORMATION



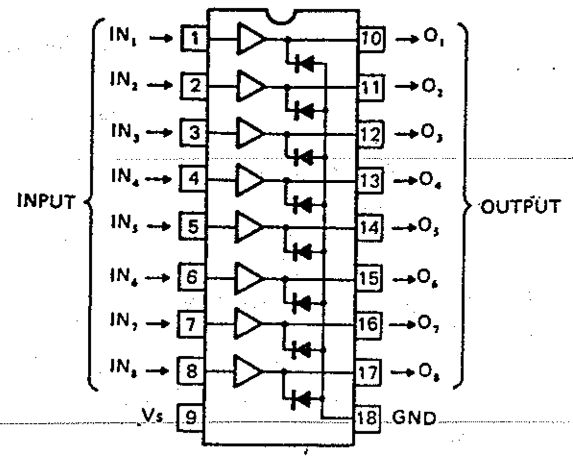
$D_0 \sim D_7$: Data Bus (8 bit)
CLK N : Counter Clock Inputs
GATE N : Counter Gate Inputs
OUT N : Counter Output
RD : Read Counter
WR : Write Command or Date
CS : Chip Select
$A_0 \sim A_1$: Counter Select

μPD8253C-5
PROGRAMABLE INTERVAL TIMER

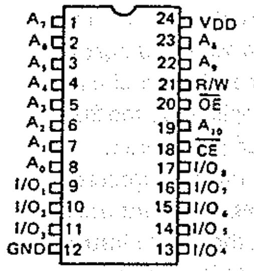


(1) For total compatibility and upgradability from the 2732A and ROMs provide a trace to pin 26.

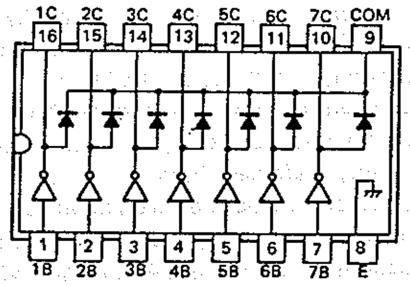
2764
(8K x 8) UV ERASABLE PROM



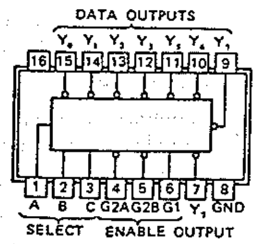
M54563P
8-UNIT 500mA SOURCE TYPE
DARLINGTON TRANSISTOR ARRAY



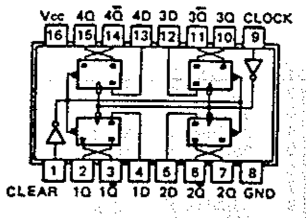
TC5517AP
(2048 x 8)
CMOS STATIC RAM
(or MSM 5128-15RS
or MB 8417A-15)



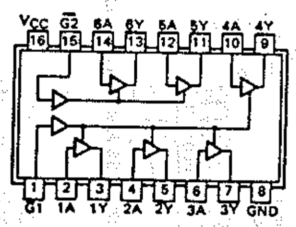
ULN2003A
DARLINGTON TRANSISTOR ARRAYS



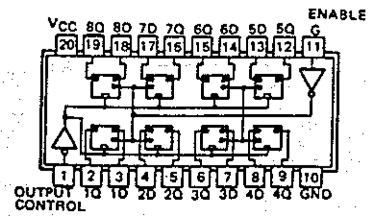
SN74LS 138
3-TO 8-LINE DECODERS/MULTIPLEXERS



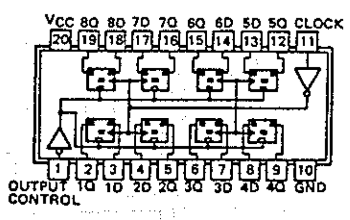
SN74LS 175
QUAD D-TYPE FLIP-FLOPS



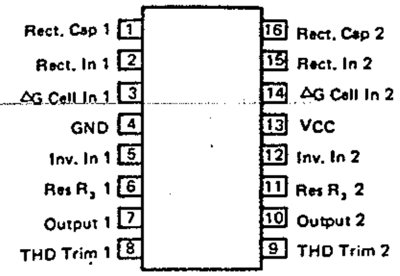
SN74LS 367
HEX BUS DRIVERS



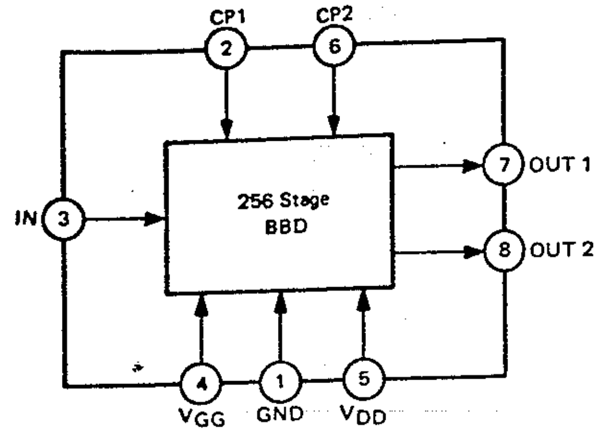
SN74LS 373
OCTAL D-TYPE LATCHES



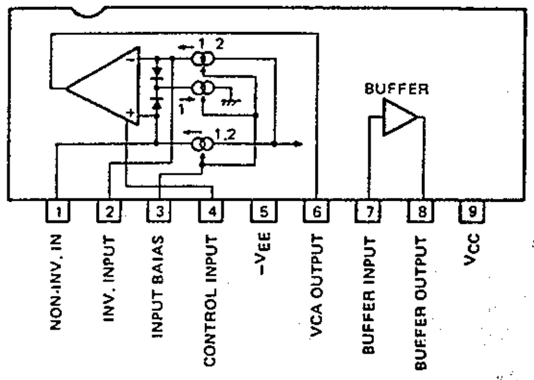
SN74LS 374
OCTAL D-TYPE FLIP-FLOPS



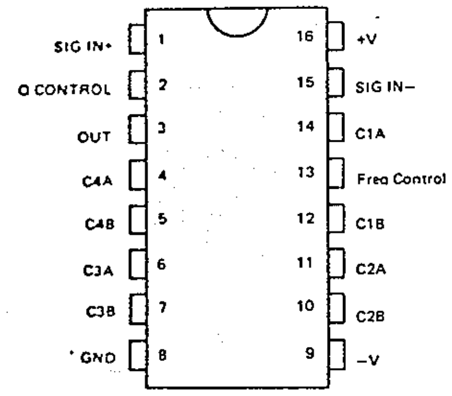
NE571N
COMPANDOR



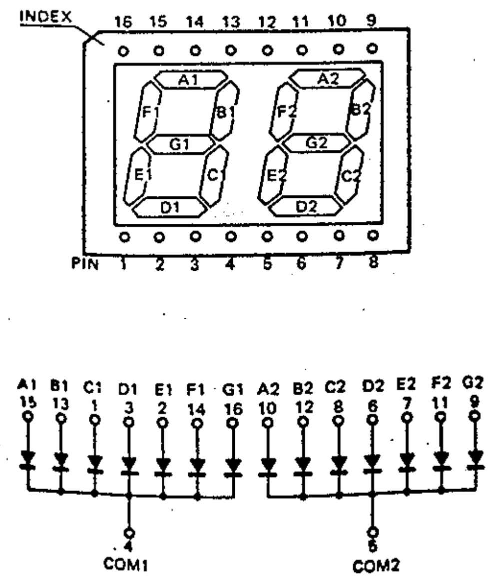
MN3009
256-STAGE BBD



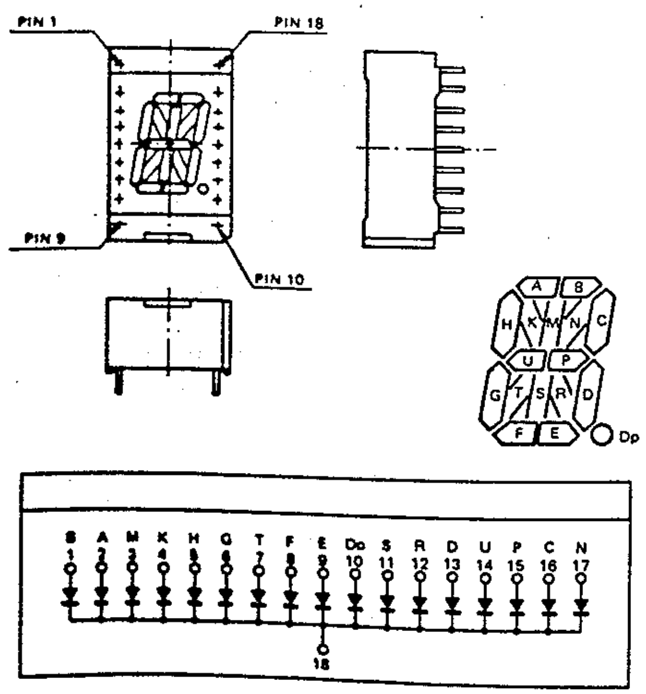
BA6110 V.C.A.



SSM 2044
4 POLE VOLTAGE CONTROLLED FILTER

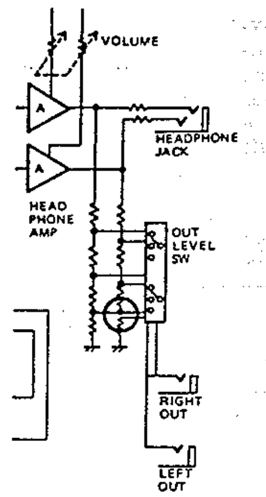
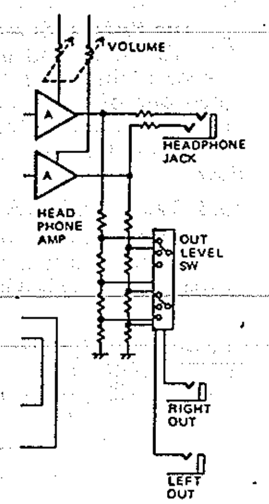
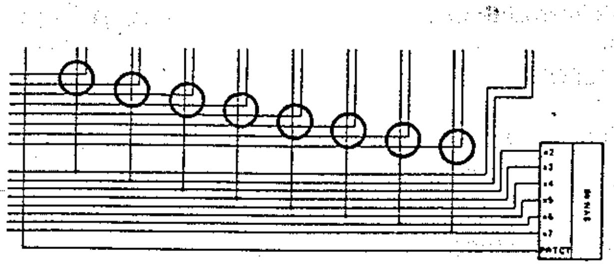
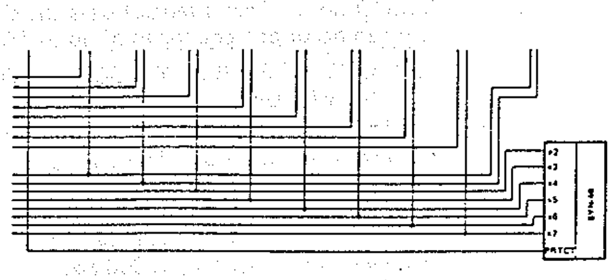
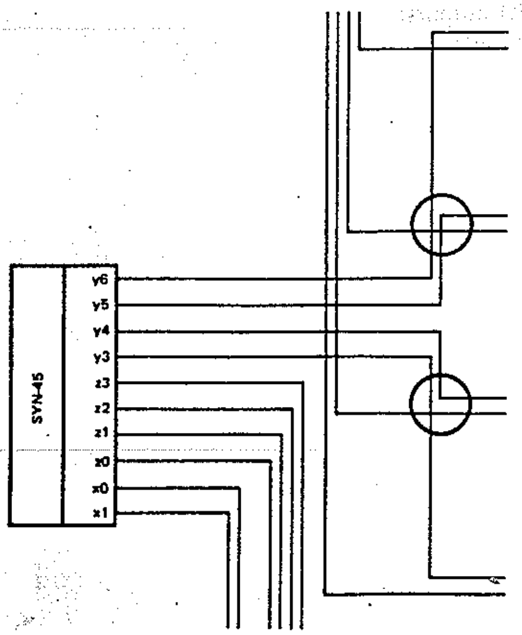
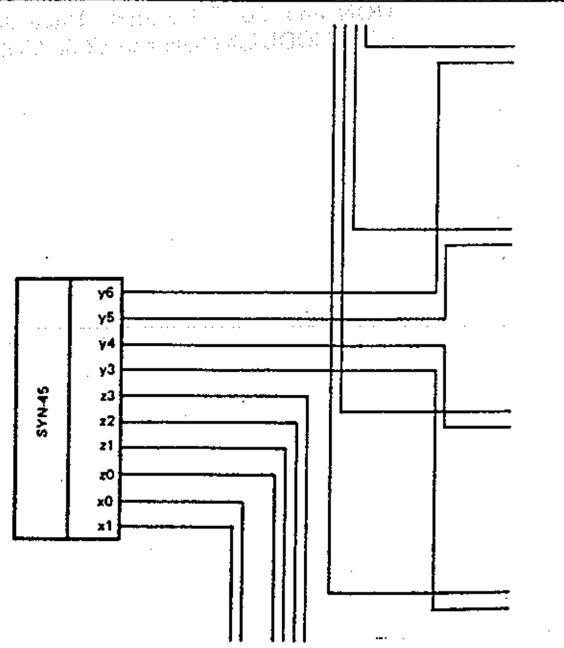


LB-402



TLR-370

ERRATA SX-210 Service Manual

Page	Error	Correction
7		
13-21		Additional illustrations Page 13  Page 21 
22	– Notes – 1. Unless otherwise specified, all transistors (Q17-24) are Part No. 2SA780.	– Notes – 1. Unless otherwise specified, all transistors (Q17-24) are Part No. 2SA798.
29		
32		

9. MICROCOMPUTER (SYN-42)

The core of the microcomputer is the component I23, the central processing unit (CPU), a 8051-series 8-bit microprocessor. The pins 00–07 (AD0–AD7) output the multiplexed data and lower half of the address to the DATA and ADDRESS BUSes, while the next eight pins (20–27) output the upper half of the address (A8–A14). The component I20 separates out the lower half of the address (A0–A7) from the multiplexed data (AD0–AD7).

9.1 PROGRAM

The SX-210 program is stored in the component I16 (Part No.2764), an 8-kilobyte erasable programmable read-only memory (EPROM). The CPU follows the instruction steps contained in this program.

9.2 STORAGE

The computer's 2 kilobytes of main storage is located in the component I12 (Part No.5517). This battery-protected ROM [?] acts primarily as the TONE MEMORY, but also serves as a work area for the CPU.

9.3 DIGITAL-ANALOG CONVERTER

Components I26, I27 (combined in Part No.CD4049), and I29 (Part No.TL082), together with the ladder network built up of 10 kOHM and 20 kOHM resistors, form a 10-bit digital-analog converter which outputs, on a time-shared basis, the voltage outputs from the CPU's output port (pins 10–17). This output is used primarily as the voltage output of the SAMPLE & HOLD function. It is also fed into the component I28 (Part No.TL080) to form an 8-bit analog-digital converter for the PITCH BENDER circuits.

9.4 500 Hz OSCILLATOR

The two inverter gates (I18) form a 500 Hz oscillator, the output of which is connected to one of the CPU's interrupt terminals (pin 33) to flash all the LEDs on the SX-210 panel.

9.5 480 kHz OSCILLATOR

The other oscillator in the component I18 provides the components I4 and I5 (both Part No.8253(2M)) with the master clock signal for the envelope generators.

9.6 MASTER OSCILLATOR

The circuit containing the transistors Q1 and Q3 generates the master frequency (approximately 4 MHz) for building sounds.

9.7 DCO PULSE GENERATOR

Together, the components I1, I2 and I3 (Part Nos.8253 (2M)/(4M)) generate the DCO PULSE from data supplied by the CPU. The pulse outputs (DC0–DC7) are then fed into the SAWTOOTH GENERATOR on circuit board SYN-43.

9.8 SHIFT CIRCUITS

The components I7 and I8 (both Part No.ULN2003AV) shift the input voltages—EG PULSE and KEYING SIGNAL, respectively—from 0 vs. +5V to 0 vs. +15V.

9.9 PULSE INPUT PORTS

The components I10 and I14 (both Part No.LS367) are input ports for the pulses returning from the KEYBOARD, PANEL, and INCREMENTER.

9.10 KEY SCAN

The component I17 (Part No.LS138) generates the SCANNING PULSEs sent to the keyboard. Pulses returning from the keyboard signal the program to generate a sound.

9.11 DELAY CIRCUIT

The eight elements of the components I21 and I22 (Part Nos. CD4001 and CD4011, respectively) form a monostable vibrator which momentarily blocks the output and thus eliminates shock noise when changing tones.

9.12 CASSETTE INTERFACE

The component I25 (Part No.TL211) is an amplifier which converts data from the cassette player into the digital form.

9.13 CASSETTE INTERFACE

The transistors Q2 and Q4 (Part Nos. A564 and C536) cut in the battery to protect the contents of the TONE MEMORY when the power supply is turned off.

10. PROGRAM

10.1 SOUND GENERATION

The first stage of the program is a KEY SCAN. The component I17 (Part No.LS138) sends out eight consecutive pulses to each group of eight keys in order from the lower end of the keyboard through the circuits marked KS0–KS7.

Note: KS7 is attached to only five keys so the component sends only five pulses.

If none of the keys are depressed, none of these pulses return to the components I10 and I14 (both Part No. LS367). The microprocessor repeats the scan until receives such a pulse.

When, however, a key is pressed, the returning pulse signals the processor to compute, from the pulse timing, which key has been pressed. The relevant frequency data for that key then goes to an open channel selected from the 8 provided by the components I1, I2 and I3 (Part No.8253). It is the channel which outputs the actual frequency. At the same time, the computer directs the component I8 (Part No.ULN2003AV) to start issuing the KEYING SIGNAL for the channel so that the circuit board SYN-43 can generate the sound.

10.2 REGENERATING THE SAMPLE & HOLD DATA

The SAMPLE & HOLD circuit forms the interface between the digital circuits of the microcomputer and the analog circuits generating the sound output. The program sets the 31 condensors in the SAVE & HOLD circuit by inputing the data stored in digital form in the EPROM I26 (Part No.2764) and outputing it sequentially, on a time-shared basis, through the digital-analog converter made up of the components I26 and I27 (combined into Part No. CD4049). However, with the passage of time, the charge on the condensors fades. Therefore, the computer must repeat this process at regular intervals to regenerate the data.

Note that this data differs for each tone. When the tone is changed, the computer completely replaces all data in the SAMPLE & HOLD condensors.

10.3 INCREMENT

The INCREMENT knob on the panel, as is readily evident from the SYN-45 circuit diagram, is connected to only two switches. The position of this knob determines the relative timing with which these two switches turn on. The component I14 then outputs this parameter to the computer.

If the increment knob is off the mid-position, this parameter is non-zero so the computer adjusts the output to the synthesizer. The change in parameter then produces a change in tone.

10.4 PITCH BENDER

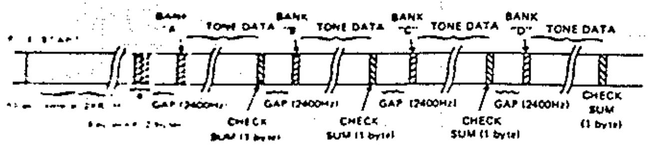
The PITCH BENDER is connected to a self-restoring rotating rheostat. The analog-digital converter—made up of the component I28 (Part No.TL080), the ladder network of 10- and 20-kOHM resistors, and components I26 and I27 (combined into Part No.CD049)—changes the electrical analogue of the rheostat position to a digital input for the computer. This converter is programmed for sequential comparisons. The computer, once it has this information, calculates the proper frequency to be added to the waveforms of each channel.

10.5 PANEL SCAN

The PANEL SCAN is essentially the same as the KEYBOARD SCAN and immediately follows it. The only difference is that only one switch can be pressed at a time. When one of the panel switches is pressed, the computer immediately alters the corresponding section of the program flow. Otherwise, it simply proceeds with the current flow.

10.6 TAPE INTERFACE

The hardware component of the tape interface consists of only the circuitry centered on component I25. The bulk of the formatting is handled by the computer program.



The data transfer itself only takes about 20 seconds.

11. INTERRUPTS

The SX-210 uses three different types of interrupts. In order of decreasing precedence, they are:

11.1 LED INTERRUPT

All LEDs on the panel flash at the frequency of 500 Hz provided by the oscillator in component I18. This interrupt keeps the LED from flickering.

11.2 PORTAMENTO/GLISSANDO INTERRUPT

This interrupt occurs only for PORTAMENTO/GLISSANDO notes. This interrupt uses the CPU's internal timer so it can occur at frequencies of up to 5 kHz.

11.3 LOW FREQUENCY OSCILLATOR (LFO) INTERRUPT

The low frequency oscillator function is handled entirely with interrupts. The only physical correlate is the output terminal to the SAMPLE & HOLD circuit.

This interrupt, too, uses the CPU's internal timer, but the frequency is controlled by the LFO SPEED setting. The maximum frequency is 300 Hz.

Processing affected includes DELAY, VIBRATO, PITCH BENDER, VCF MODULATION, VCA MODULATION and EG TRIGGER. There are two LFO outputs: VCF MODULATION and VCA MODULATION (S/H).

■ CIRCUIT FUNCTIONS

1. SAMPLE & HOLD (SYN-43 CIRCUIT DIAGRAM (1/2))

Components I11–I14 (Part No.CD4051BE) are multiplexers which distribute the SYN-42 digital-analog converter time sharing data.

The transistors Q_1 and Q_2 form an antilog circuit which converts a linear input into a logarithmic output. The component 1/2 I2 (Part No.TL082) then converts the output current value into a voltage, which is negative.

A zener diode supplies a −10V power supply at pin 7 of I11.

Also attached to pin 3 on the I11 component is a WZ-081 component which serves to protect the integrated circuit.

The 1/2 I2 (Part No.TL082) circuit below the antilog circuit is an adjustable temperature compensation amplifier. Its primary function is to compensate for the differences in resistance produced by temperature changes.

Further down is the KCV amplifier built around the component I3 (Part No.BA6110). Even when the KCV LEVEL is zero, pin 1 outputs the time sharing information from this component to the channels. The component is current-regulated through pin 4 so it has a transistor (Q3) which converts voltage into a current. The base voltage has sufficient bias to ensure that the input-output characteristics are linear even when the emitter voltage (the input) is in the vicinity of zero.

The input to I13 (Part No.CD4051BE) comes directly from the digital-analog converter so is not temperature-dependent.

The SAMPLE & HOLD output from pin 13 passes through a low pass filter made up of a 1-kOHM resistance, a 1 uF capacitance, and a 1/2 I107 (Part No.NJM4558). This filter smooths out pulse width modulation (PWM) waveforms with high low frequency oscillator (LFO) frequencies to eliminate noise.

The VCF CUTOFF and low frequency oscillator (LFO) outputs from the I14 multiplexer (pins 13 and 14, respectively) are mixed to yield a single output FLFO.

The two diodes attached to pin 12 on the I14 moultiplexer are to prevent the envelope generator from oscillating when the sustain level becomes negative.

The output from the component I10 (Part No.CD4050 BE) is not linear, but digital, alternating between 0 and 5V. Since theCMOS IC has a high input impedance, this output acts as a latch.

2. NOISE GENERATOR (SYN-43 CIRCUIT DIAGRAM (1/2))

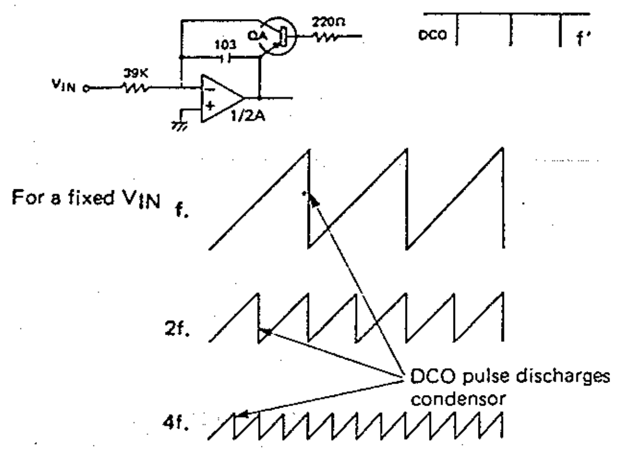
This circuit uses two 1/2 I28 (Part No.TL082) components to amplify, in two stages, the noise generated by applying a reverse bias between the base and emitter of the transistor Q8.

3. SAWTOOTH GENERATOR (SYN-43 CIRCUIT DIAGRAM (2/2))

As mentioned earlier, the input voltage (V_{in} in the accompanying Figure) applied to the 39 kOHM resistor is negative. This means that the operational amplifier (OP AMP) output rises at a rate proportional to this voltage value.

Each time a pulse from the 16-bit DCO PULSE GENERATOR (Part No.8253) on circuit board SYN-42 reaches the base of transistor QA, it short-circuits the collector and emitter so that the condensor discharges and the operational amplifier (OP AMP) outputs starts rising from 0V once more. (see Figure 1)

Two 10 kOHM resistors divide this output in half for output to the ANALOG SWITCH (1/4C: Part No. CD4066). This terminal is also clamped through a diode to the voltage output from the 1/2 I1 (Part No. NJM4558). This clamping not only protects the ANALOG SWITCH but also blocks large amplitude waveforms formed when the frequency suddenly changes, producing a phase difference between the outputs of the timer and the SAMPLE & HOLD circuit.



For a fixed V_{IN}, the slope remains constant. As a result, the amplitude decreases in inverse proportion to the relative frequency. Therefore, V_{IN} is made proportional to the frequency.

<Figure 1>

4. PULSE WIDTH AND SUB OSC (SYN-43 CIRCUIT DIAGRAM (2/2))

The other 1/2 A (Part No. NJM4558) is a comparator. The sawtooth waveform from its noninverting (NON INV) terminal and the SAMPLE & HOLD output from its INV terminal are combined to produce the pulse width modulation (PWM) output. This output in the range ±15V is reduced with 240 kOHM resistor. The S/H (PW) output is divided with a 39 kOHM and 47 kOHM resistor. This output provides a bias so that the PMW output has the same mean value for all values of PULSE WIDTH.

The component 1/2 B (Part No.4013BE) is a frequency divider which outputs a square wave with a frequency half that of the digitally controlled oscillator (DCO). The integrating circuit between the oscillator and this component (made up of a 100 kOHM resistor, a diode, and condensor #101) uses the base capacity of the transistor QA to assure correct operation.

5. VOLTAGE CONTROLLED FILTER (VCF) (SYN-43 CIRCUIT DIAGRAM (2/2))

Central to the VCF circuit is the ID component (Part No.SSM2044).

Pins 1 and 15 are for the noninverting (NON INV) and INV inputs, respectively. Both inputs are grounded through 470-ohm resistors to provide bias.

Pins 2 and 13 control the RESONANCE and CUTOFF frequencies, respectively. These inputs can be linear because the ID component incorporates linear-antilog converters. The cutoff frequency changes approximately 10 octaves for every 1V change in the output of the 1/2 E (Part No. NJM4558), a component which simultaneously mixes the outputs of the SAMPLE & HOLD CUTOFF, SAMPLE & HOLD KEY CONTROLLED VOLTAGE (KCV), and VCF envelope generator and reverses the polarity of the output waveform.

The output from ID component (pin 3) is a current. A second 1/2 E (Part No.NJM4558) converts this into a voltage supplied to the check pin of each channel.

■ PARTS LIST

235740	SYN-42 (1)		
235741	SYN-43 (1)		
235742	SYN-45 (1)		
235743	SYN-46 (1)		
235744	FH-07 (1)	JAPAN	
235745	FH-07 (2)	CEE, SAA	
235746	FH-07 (3)	OTHERS	
235747	FH-07 (4)	USA	
235748	FH-07 (5)	CSA	
235753	FH-07 (6)	NE	
235749	SYN-44, 47, PS-33, JA-06 (1)	JAPAN	
235750	SYN-44, 47, PS-33, JA-06 (2)	USA	
235751	SYN-44, 47, PS-33, JA-06 (3)	CEE, SAA, NE	
235752	SYN-44, 47, PS-33, JA-06 (4)	CSA	
708028	BATTERY	GB50-3	
800084	POWER TRANS	TSE-218D	
	POWER TRANS	TSE-218U	
	POWER TRANS	TSE-218I	
	POWER TRANS	TSE-218E	
710368	VOLUME	GM70E 50KB	
713616	POWER SWITCH	WK2A44	
787302	KNOB	RVT-4	
787422	KNOB	SVT-4 (YELLOW)	
800079	KNOB	RVT-10	
787329	SENSOR LEVER		
787376	CODE WINDER		
789322	SHIELDED CODE	2.5M	
800078	SW. GUARD		
800080	VOICE PLATE		
800081	NUMBER COVER		
800073	C-SCALE KEYBOARD	ESK-7013	
	C KEY		
	D KEY		
	E KEY		
	F KEY		
	G KEY		
	A KEY		
	B KEY		
	TOP-C KEY		
	# KEY		
800094	DATA CASSETTE TAPE		
900215	SIDE BOARD (RIGHT)		
900220	SIDE BOARD (LEFT)		

SYN-42

706025	IC	C-MOS 4001 BP
706029	IC	C-MOS 4069
706039	IC	CD 4011
706069	IC	TL 082CP
706080	IC	C-MOS 4049B
706085	IC	TL 080
706102	TRANSISTOR	2SA564R
706123	TRANSISTOR	2SC536G
706544	Z. DIODE	WZ-052
706917	IC	SN74LS367N
706929	IC	SN74LS373N
706939	IC	SN74LS138
706986	IC	8253C-5
706996	IC	MB74LS374
710412	OSC COIL	25MH
800044	RESISTER	RM 8-332J
800046	IC	P8031
800047	IC	MSM5128-15RS
800048	IC	TC40H032P
800049	IC	ULN2003A
800050	IC	TL311P
800053	X-TAL	HC18/U12.000MHZ
900841	IC 2P25A	MBM2764-25
706301	DIODE	1S2473

SYN-43

706025	IC	C-MOS 4001 BP
706032	IC	C-MOS 4081B
706042	IC	C-MOS 4013B
706051	IC	C-MOS 4050B
706069	IC	TL082CP
706077	IC	NJM-4558DD
706102	TRANSISTOR	2SA564R
706123	TRANSISTOR	2SC536G
706141	TRANSISTOR	2SA798
706301	DIODE	1S2473
706502	Z. DIODE	WZ-100
706511	FET	2SK44D
706937	IC	BA6110
800051	IC	CD4066 BE
800056	IC	SSMT2044
800057	Z. DIODE	WZ-081
800140	IC	CD4051 BE

Adjustment	Voice Identifier	Procedure
6. VCF OFFSET RESONANCE adjustment	RESON 1 ~ 8	Note: Set the parameters to the follow values: VCF CUTOFF 50 RESONANCE 98 MOD (KCV, LFO, EG) 0 KEY all off and C1 (CH.1) only 1. After setting the tone memory switches to A-1, examine the SYN-43 check pin #8 trace on an oscilloscope set to its maximum range. 2. Turn the VCF OFFSET (CH.1) adjuster (#7) until the waveform (or trace) is centered on the 0V line. 3. After turning the VCF RESONANCE LEVEL (CH.1) adjuster (#23) counterclockwise to start the signal, turn it clockwise to the exact level at which the signal stops. 4. Repeat the above procedure for the A-2 through A-8 tone control settings (connecting the oscilloscope to check pins #9 – #15 and using the corresponding of adjusters) to adjust all eight channels.
7. VCF CUTOFF (CH.1) adjustment	CUTOF 1	Note: Set the parameters to the follow values: VCF CUTOFF 50 RESONANCE 99 MOD (KCV, LFO, EG) 0 1. After setting the tone memory switches to A-1 and the SUB OSC switch to ON, write into A-1. 2. With the oscilloscope attached to check pin #8 on the SYN-43 circuit board, turn the VCF CUTOFF (CH.1) adjuster (#15) on the SYN-43 circuit board until the amplitude is at its maximum. 3. Set the tone memory switches to B-1 and make sure that the pitch is still approximately the same when heard through the monitor amplifier.
8. VCF CUTOFF (CH2–CH8)	CUTOF 2 ~ 8	1. Connect the SIGNAL OUT terminal to the monitor amplifier. (Or, alternatively, use a headphone.) 2. Change the tone memory switches to B-2 to compare channels 1 and 2. Turn the VCF CUTOFF (CH.2) adjuster (#16) on the SYN-43 circuit board until the pitches agree. 3. Repeat this process for channels 3 through 8, changing the tone memory number and turning the appropriate VCF CUTOFF adjuster (#17 – #22).
9. KCV LEVEL adjustment	KCV-99	Note: Set the parameters to the follow values: C-1 Signal generators all OFF VCF CUTOFF 50 RESONANCE 99 LFO EG 0 Oscilloscope range 200 μsec/div 1. Set the tone memory switches to B-1 and observe the waveform at check pin #4 on the SYN-43 circuit board. 2. Adjust the oscilloscope until one wavelength occupies eight (8) divisions on the horizontal scale. 3. Change the tone memory switches to C-1 and turn the KCV LEVEL adjuster (#3) on the SYN-43 circuit board until one wavelength occupies one (1) division on the horizontal scale. Note: It is also possible to tune by ear until C-1 is three octaves higher than B-1. However, in this case, it is necessary to check the intervals by striking each key in order from the lower end of the keyboard.

Adjustment	Voice Identifier	Procedure
10. ANTILOG AMP adjustment	PLSWIS	1. After setting the tone memory switches to C-2 and connecting the SYN-43 check pin #4 output to the oscilloscope, turn the ANTILOG OFFSET adjuster (#1) until the duty is 50%. Note: Use the 200 μsec/div range of the oscilloscope.
11. VCA OFFSET adjustment	VCA ADJ	1. With the same connections, change memory switches to C-3. 2. Turn the VCA OFFSET adjuster (#5) until the level is at its minimum.
12. NOISE LEVEL adjustment		1. Attach a millivoltmeter to check pin #7 and turn the NOISE LEVEL adjuster (#6) on the SYN-43 circuit board until the level is -10 dBm. Note: Use a millivoltmeter. The RMS reading should be approximately 1.8 volts.
13. ENSEMBLE DEPTH adjustment		1. Connect the oscilloscope to check pin #4 on the SYN-44 circuit board and turn the ENSEMBLE DEPTH adjuster (#1) until the waveform measures approximately 2.5V peak-to-peak.
14. Signal-to-noise ratio check	MAX (C-4) BASIC (C-5)	1. With the panel VOLUME at the maximum (10), set the output level selector switch (located on the rear panel) to the +4 dBm position, and attach the millivoltmeter to the SIGNAL OUT (LEFT) socket. 2. Shift the tone memory switches between C-4 and C-5. The signal-to-noise ratio should be at least 70 dB.

■ ADJUSTMENTS (Page 51 ~ 53)

ADJUSTMENTS

Adjustment	Voice Identifier	Procedure
1. Panel check	000000 ↕ Flashing ****** JJ ↕ Flashing HH	1. Holding down the lowest C-major chord (C6-E5-G5), switch on the power. 2. Hold the chord for 1 or 2 seconds and then release. 3. All LEDs should start flashing. 4. Press each switch on the panel. 5. The corresponding LED should stop flashing. 6. If the MEMORY PROTECT switch on the rear panel is in the PROTECT position, the LED in the MEMORY WRITE switch will keep flashing even when it is pressed. 7. When the LEDs for all the switches are out, the diagnostic routine will automatically proceed to STEP 2: PITCH BEND. 8. To bypass any or all of the panel check, press the C6 key once. Use the same key to signal the end of steps 2-4.
2. PITCH BEND adjustment	OK 7E2 7E1 NO 000 NO FF3	1. Turn the PITCH BEND adjuster (#1) on the SYN-42 circuit board until the last three digits of the VOICE IDENTIFIER display read either 7E1 or 7E2. 2. Rotate the PITCH BEND lever all the way in both directions. The VOICE IDENTIFIER display should read 000 at the counterclockwise extremity and FF3 at the other. 3. Press the C6 key once to proceed to the next step. (The same applies to steps 3 & 4.)
3. MASTER OSC adjustment	000.00 ↓ 440.84	1. Set the MASTER TUNE control in mid-position. 2. Turn the MASTER FINE TUNE adjuster (#2) on the SYN-42 circuit board until the VOICE IDENTIFIER display reads in the range 440.81-440.88. Note: This is the only step requiring a turning screwdriver.
4. TEMPERATURE COEFFICIENT adjustment	SH-ADJ	1. Turn the TEMPERATURE COEFFICIENT adjuster (#2) on the SYN-43 circuit board until the voltage at check pin #2 is 4.50V. Note: Use a digital voltmeter to measure the voltage.
5. KCV OFFSET adjustment	KCV OST	1. Turn the KCV OFFSET adjuster (#4) on the SYN-43 circuit board until the waveform at check pin #1 is centered on the 0V line. Note: Use the oscilloscope's maximum voltage range. 2. Simultaneously press C6 and F#5 once to proceed to the next step. Note: The diagnostic routine will replace the contents of the 32 tone memory locations with ROM test data so SAVE the current data, if required, on tape before proceeding to the next step.

KAWAI TECHNICAL SUPPORT BULLETIN
August 31, 1983
TSB-0042

Countermeasure:

This fault can be cleared by erasing the contents of the RAM and returning them to their initial values. (Note, however, that the existing contents are lost in the process.)

Procedure:

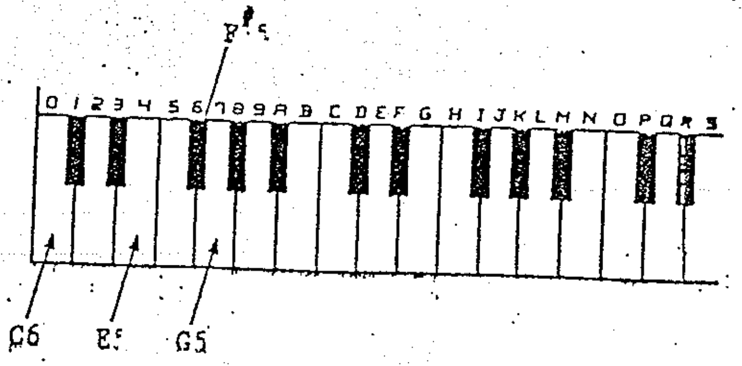
1) Turn the SX-210 OFF.

2) Reapply the power while playing the lowermost C-major chord C6-E5-G5 (see Figure 2).

3) Release the chord.

These two steps load the self-diagnostic program into the CPU (Part No.8031, I23 in Figure 1). The CPU will start by flashing every LED and indicator on the panel.

4) Press the two keys C6 and F#5 simultaneously to terminate the self-diagnostic program.



<Fig. 2>

The SX-210 will then be ready to play except that the contents of the RAM will contain test data copied from the SX-210's EPROM (Part No.2764(2P-25A), I16 in Figure 1). To restore the contents of the tone memories, use the MEMORY WRITE function or input back-up copies through the cassette interface.

TECHNICAL SUPPORT BULLETIN
August 31, 1983
TSB-0042

RESETTING THE SX-210 TONE MEMORIES

19 SEPT 1983

Subject;

We have received reports that SX-210's tone memory sometimes does not operate as it should. We hereby advise you of the problem, its root cause, and the appropriate countermeasure.

Problem:

Pressing a tone memory key--for example, C-4--sometimes returns the SX-210 to A-1 or produces tone effects different from those desired.

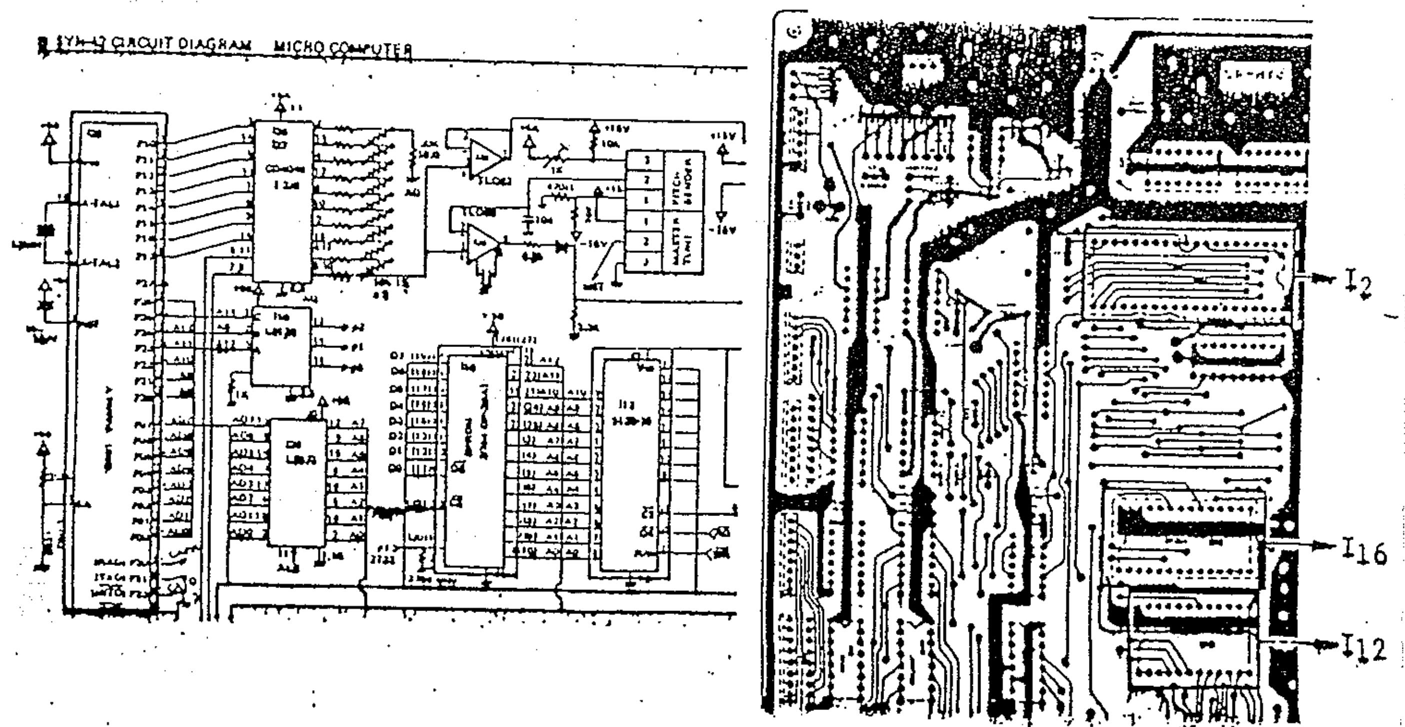
Cause:

The RAM (Part No.5128-15, I12 in Figure 1) on the printed circuit board SYN-42 contains incorrect data. This data can be written into RAM as the result of three actions;

1) external shocks

2) replacing a circuit board

3) replacing an IC, LSI, or other element on a circuit board



<Fig. 1>

TECHNICAL SUPPORT BULLETIN

T.S.B. - 0043
Sept. 13, 1983

Mistriggering in the VCA EG Circuits

Subject:

We have received reports of trouble with the SX-210's synthesizer. We hereby advise you of the problem, its root cause, and the appropriate countermeasure.

Problem:

On voices with short ATTACK, DECAY, SUSTAIN and long RELEASE, the keyboard will intermittently mistrigger and sustain the note.

Cause:

The problem lies in the VCA EG circuits on the printed circuit board SYN-43. Faulty output from IC 4066 causes the comparator (IC 4558) to mistrigger.

Countermeasure:

This fault can be removed by connecting the comparator's No.2 pin to the +15 V terminal (pin No.8) through a 4.7 MOHM resistor.
(Repeat the above for all eight (8) channels.

Note

The above modifications have already been implemented for models shipped during or after August 1983.
(Serial Nos.K-5808 and later)